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VEHICLE DETECTION PHASE III: PASSIVE BUS DETECTOR/INTERSECTION PRIORITY SYSTEM DEVELOPMENT

Option II: Manufacturing Drawings and Prototype Development

Volume I

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Operation and Maintenance Manual

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FOREWORD

This report is the result of a contract with Honeywell, Inc. to develop a Passive Bus Detector and Intersection Priority system. The system functions as a fully independent traffic controller with completely passive bus detection capability (i.e. with no special equipment required on the bus) using inductive loop detectors (ILD) placed in the roadway.

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Charles F. Scheffey
Director, Office of Research

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16. Abstract

General information regarding the installation, operation and maintenance of the Passive Bus Detector (PBD) is discussed. Installation and operation require no special adjustments except tuning the inductive-loop electronics to the loop and lead-in. When operated with a 6-ft x 6-ft loop, correct classification of mass transit (40-ft) busses should reach or exceed 95% with less than 1% false classification.

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SECTION 1
INTRODUCTION

1.1 PURPOSE

This manual contains the installation, operation, and maintenance instructions for the Passive Bus Detector (PBD) system. In addition, the manual covers general operating theory, front panel indicators and controls, and input/output functions. General information is presented to encourage the system's use where mass transit bus priority and monitoring can be used to advantage. Included in this manual are diagnostic procedures, functional module descriptions, schematics, and parts lists.

1.2 SYSTEM DESCRIPTION

The PBD is a stand-alone, microprocessor-based system for passively detecting the presence of widely used 40 to 60-ft*mass transit busses on a roadway. Although the PBD was developed to operate with busses manufactured by GMC, AMG, and Flxible, it can be adapted to other bus types and manufacturers should the need arise. The PBD uses the commonly-used inductive-loop transducer. No bus driver cooperation is required other than driving the bus over the detection zone of the loop(s).

The PBD system consists of two components: 1) a four-pack Inductive-Loop Detector Unit (ILDU) (Figure 1) and 2) a 16-channel Bus Classifer Unit (BCU) (Figure 2). Each Inductive-Loop Detector (ILD) is a high-quality detector which drives the inductive loop and extracts changes in loop inductance due to vehicle presence. In addition, it contains the vehicle and bus call relays. The system's intelligence is located in the BCU. The BCU contains two

* 1 ft. = .3048 m.

Figure 1. Inductive-Loop Detector Unit (ILDU)

Figure 2. Bus Classifier Unit (BCU)

microprocessors which process the raw detector information from a maximum of 16 ILDs (four 4-pack ILDs). The bus/no-bus decision made by the BCU is returned to the respective ILD. Figure 3 shows how these two units are interrelated.

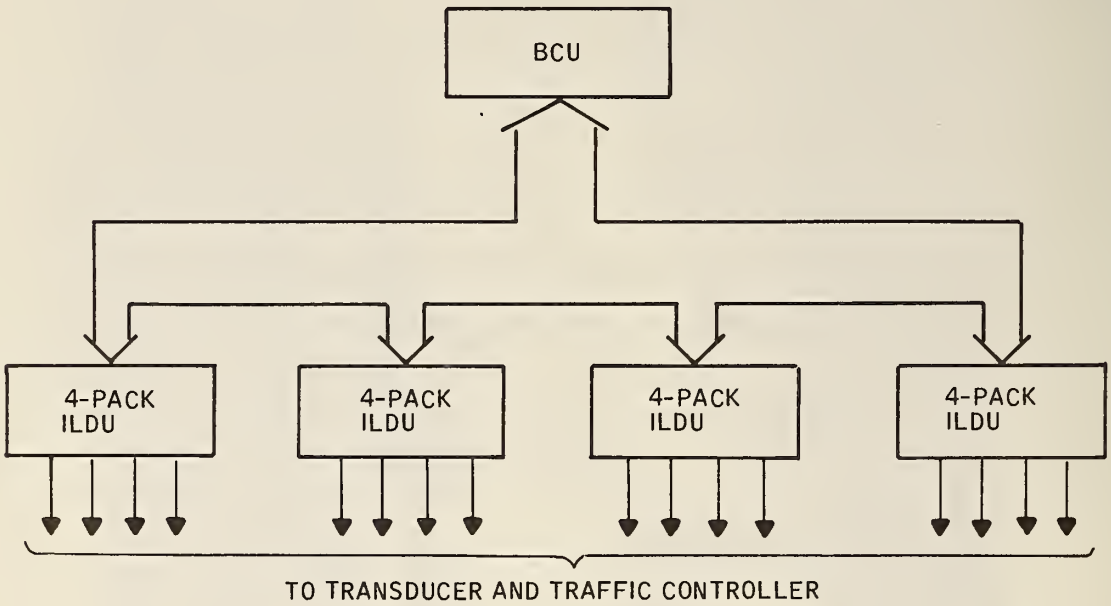


Figure 3. PBD Interconnect Diagram

1.3 OPERATIONAL CHARACTERISTICS

1.3.1 Inductive-Loop Detector Unit

The ILDU consists of a power supply section plus space for four ILDs. Each ILD is pluggable, so that a system which requires a nonmultiple of four ILDs must install only the number of ILDs needed. The power supply section also contains the relays for interfacing with the traffic controller.

1.3.1.1 Outputs -- One set of relay contacts (N.O., N.C., Common) for vehicle call. One set of relay contacts (N.O., N.C., Common) for bus call for each detector. Contacts rated at 2.0 amperes.

1.3.1.2 Controls -- Tuning; Vehicle call duration (short, medium, long); Sensitivity adjust.

1.3.1.3 Indicators -- Coarse tuning; Output signal monitor; Tune limit.

1.3.1.4 Inductive Loop -- Three-turn, 6-ft x 6-ft*; lead-in = 360 ft* maximum; series/parallel combinations not permitted.

1.3.1.5 Power Requirements -- 110 Vac, 60 Hz, 1.0 ampere.

1.3.1.6 Mounting -- Shelf - width 13.5 in.*, height 6.5 in.*, depth 6.9 in.* (with cable connectors); weight 10 lb.*

1.3.2 Bus Classifier Unit

The BCU is the device which receives a vehicle signature from the ILD and analyses the signature's shape. If the signature belongs to that of a bus, the BCU issues a signal to the ILD which, in turn, initiates a bus call to the controller.

1.3.2.1 Inputs -- Up to 16 simultaneous vehicle signatures, 0 to 10 Vdc; Remote reset.

1.3.2.2 Outputs -- Up to 16 vehicle and 16 bus classification event signals, transistor-transistor logic (TTL) compatible, "Low True" logic level; Fault 1, 2 and 3 outputs, TTL open collector, "Low True" logic level. (zero volts = logic 1)

* 1 ft. = .3048 m., 1 in. = 2.54 cm., 1 lb. = .4536 kg.

1.3.2.3 Power Requirements -- 110 Vac, 60 Hz, 2.0 amperes.

1.3.2.4 Controls -- System Clear; Test.

1.3.4.5 Indicators -- Fault 1, Fault 2, Fault 3.

1.3.4.6 Mounting -- Shelf-width 20 in.*, height 7.8 in.*; depth 10.1 in.* (with cable connectors); weight 15 lb.*

1.3.3 General

1.3.3.1 Classification Range -- Vehicle centerline to loop centerline ± 4 ft.*

1.3.3.2 Vehicle Detection Range -- Variable with sensitivity setting on ILD.

1.3.3.3 Environmental Characteristics -- Operating temperature range -30°F to +165°F; humidity range to 95 percent noncondensing relative humidity.

1.3.3.4 Loop Placement-- Bus classification takes place only after the bus has completely passed over the loop. Therefore, the loop should be placed at least one bus length back from the stop bar.

1.3.3.5 Classification Accuracy -- Classification accuracy for AMG, Flxible and GMC busses in a mixture is greater than or equal to 95 percent.

1.3.3.6 False Classification -- This parameter, defined as the ratio of non-busses classified as a bus, to the total number of vehicles, is less than 1 percent.

* 1 in. = 2.54 cm., 1 lb. = .4536 kg., 1 ft. = .3048 m.

SECTION 2
PBD/CONTROLLER APPLICATIONS

2.1 INTRODUCTION

This section covers the application of a Passive Bus Detector (PBD) system to typical existing or proposed traffic signal controller installations.

Each application of a PBD to a traffic signal control installation will or will not require additional peripheral control circuitry. This will depend on the type of equipment being used for control and also the control strategy being used at the particular installation.

Material in this section is to be used as a guide in determining what, if any, peripheral equipment is required and also to illustrate some typical applications. In each individual case of actual application, the user should first determine with what controller he is going to use the detector-classifier, the strategy he is going to use, and then consult with his own technical staff or the manufacturer of the controller to determine the need for additional specific hardware and what equipment modifications have to be made to achieve the desired results.

The PBD is exactly what its name implies. It produces a relay closure upon detection of a bus or other specified vehicle for which it has been designed. In addition, a second set of contacts produces a relay closure upon detection of all vehicles, including those classified as the specified vehicle.

In this sense, the detector-classifier combination is essentially a vehicle detection system which is capable of detecting vehicles, with the added feature of being able to produce additional detection of a specific type of vehicle.

2.2 APPLICATIONS

Figure 4 is a block diagram of the PBD.

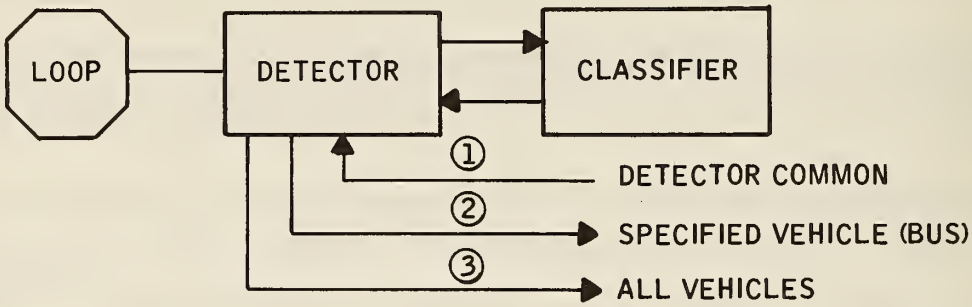


Figure 4. Passive Bus Detector Block Diagram

In detector applications of any type of vehicle detector at a traffic control installation, two connections (ref. Figure 4) are made to the detector for control purposes: the detector common (1) and the detection signal (3).

The detector common is generally the logic common or the control circuit ground of the controller or other peripheral device to which the detector is to be connected.

In the case of the vehicle detector circuits on most actuated equipment, the detection circuit (3) is connected to the detector input to the signal phase control for the phase it is to service.

This leads us to the simplest application of the PBD and one that would require no additional peripheral equipment. This application and three others are discussed next in the form of four example situations.

2.2.1 Situation 1

Assume a straight, two-phase intersection with an actuated, three-phase controller with no separate turning lane. See Figure 5.

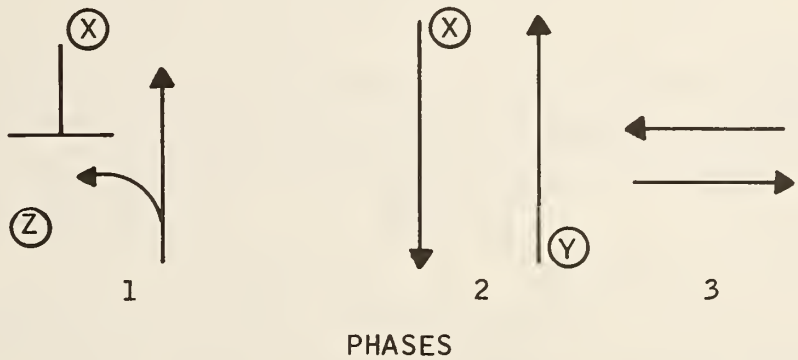


Figure 5. Situation 1 Street/Phasing Diagram

2.2.1.1 Problem -- A left-turn phase must be provided once each cycle with or without the presence of a left-turning vehicle requirement due to the heavy straight-through flow, X and Y, of the street. This turn phase is required so as not to cause long delays to a specified turning vehicle, Z, when it is present.

2.2.1.2 Results -- Because of the time used by the left-turn phase (phase 1), green efficiency is low at the intersection, and unnecessary delays are caused to straight-through vehicles at X whose desired path is in conflict with the left-turn movement Z.

2.2.1.3 Solution -- By installing a PBD and detecting the specified vehicle, Z, the left-turn phase can be eliminated except in those particular cycles where a demand is required for phase 1.

Figure 6 indicates a typical hookup of the described application.

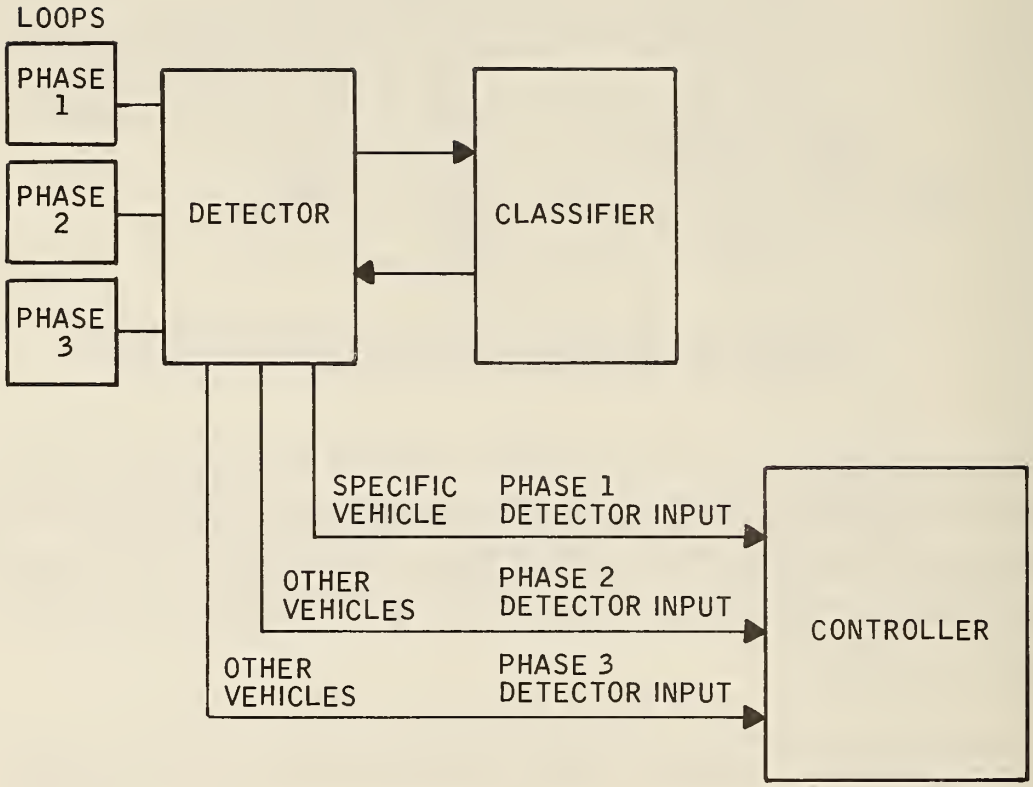


Figure 6. Solution 1 Hookup Block Diagram

2.2.2 Situation 2

A two-phase intersection with a fixed-time-interval controller such as of the state-of-the-art design (i.e., Eagle "EF", Crouse-Hinds "PCE", Econolite Type "F", Honeywell HMC-1000).

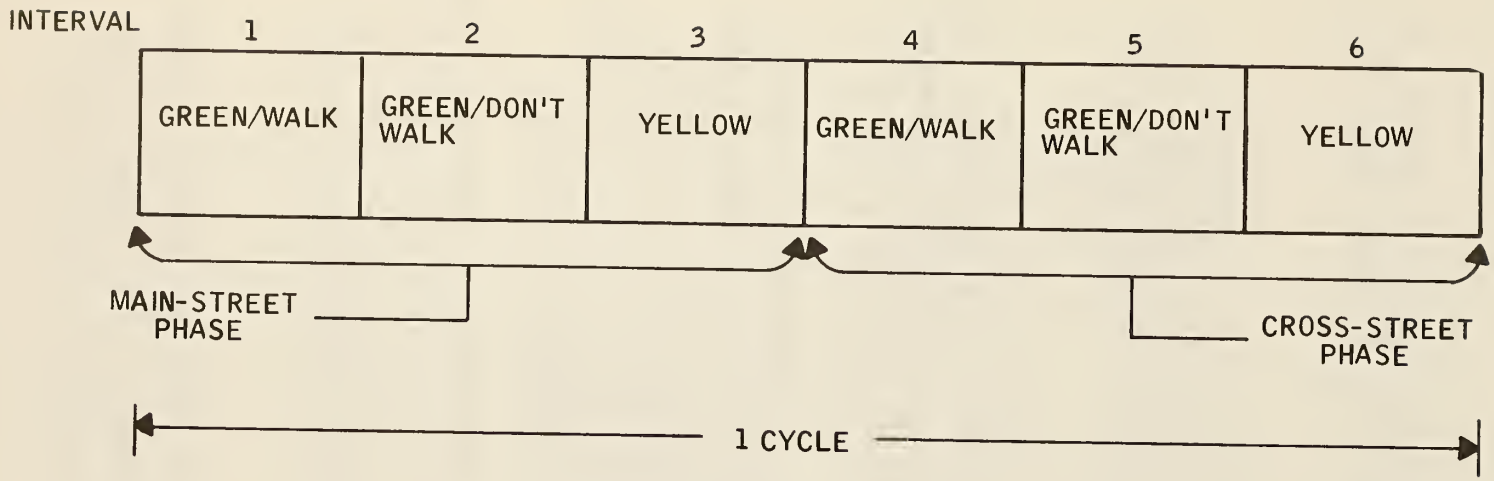
2.2.2.1 Problem -- It is desirable to cause the cross-street phase to terminate early to service an arriving bus on the main street or the main-street phase to delay termination of its phase green for some period "T" upon detection of a bus.

2.2.2.2 Solution -- In addition to a bus classifier, a bus preemption device must be added to the intersection controller to cause the desired operation. In addition, a small modification must be made to the existing controller.

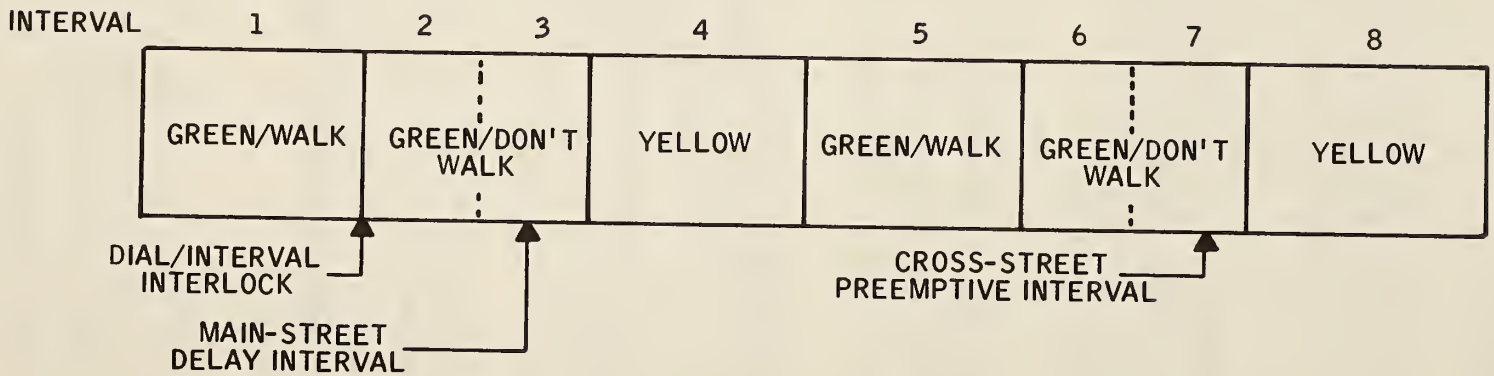
2.2.2.3 Controller Operation -- The current cycle/interval operation of the controller is shown in Figure 7A. The cycle of the controller is made up of six intervals. To enable a bus preemption operation for the main street, one approach would be to change the controller from six intervals to eight intervals as shown in Figure 7B. The intervals shown would be the "Main Street Delay Interval" and "Cross-Street Preemptive Interval."

During intervals 2 and 3, and 6 and 7, the signal displays would be the same for both intervals of their respective streets. Interval 3 would normally be set from 2 to 4 seconds in duration. Interval 7 would be set for the maximum allowable time that the cross-street phase can be shortened for the presence of a bus.

The one restriction in timing is that interval 6 must have enough time for the minimum time to clear pedestrian and interval 7 time cannot be considered as part of the clearance. Operation would be as follows (refer to Figure 7B and Figure 8):



A. Six-Interval Controller



B. Eight-Interval Controller

Figure 7. Situation 2 Controller Cycle/Interval Diagram

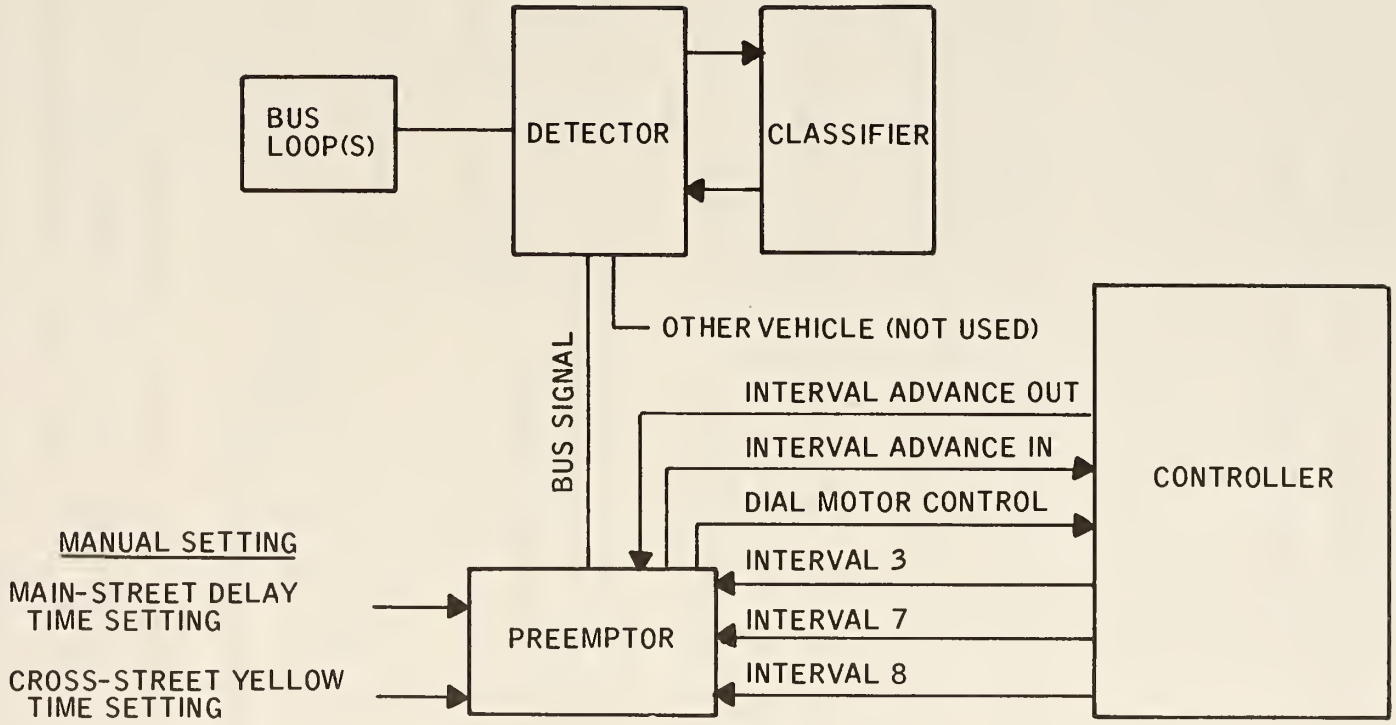


Figure 8. Solution 2 Hookup Diagram

As the controller cycles through its intervals in order and reaches interval 3 with a bus detection present, the preemptor would cause the dial motor of the controller to stop. It would stay in this condition until the bus cleared the detection zone, or a maximum delay timer times out, whichever comes first. The maximum delay would be set on the preemptor and be called the "Main Street Delay Setting." Upon either the delay timing out or the bus leaving the zone, the preemptor would restart the dial motor and the controller would continue to time.

Again as the controller cycles through its intervals and interval 7 is reached with a bus in the detection zone, the preemptor will set an advance pulse to the controller to cause it to advance to cross-street yellow.

The preemptor will time the duration of the cross-street yellow and send another advance pulse at the end of this period of time to cause the controller to go to main-street green and walk.

Since the interval is now out of step with the dial, the controller will dwell at the dial/interval interlock point (Figure 7B) until the dial gets back in step with the interval device. When this occurs, the controller will run normal until the next detection of a bus during either intervals 3 or 7.

2.2.2.4 Controller Modifications -- Controller modifications (refer to Figure 8) would be to bring out the normal interval advance circuit between the dial and interval device to the preemptor. Bring out dial motor control so that the dial can be made to dwell.[1]

Signals from the output of the controller indicating to the preemptor when it is in interval 3, 7 or 8 are required. The requirement for interval 8 is to ensure that the controller did in fact step to yellow after the preemptor sent an advance pulse.

[1] This is not required on some solid-state pretimed controllers such as the Honeywell HMC-1000, as the dial and interval are always in step and the cycle is essentially timing a series of interval times.

It should be again noted that the particular hookup described here is purely functional, and, before actual hookup on any controller is performed, the user's Technical Support group or the equipment manufacturer should be consulted on the correct hookup for a particular controller.

2.2.3 Situation 3

A multiphase-actuated intersection with three or more phases, such as a NEMA TS1-76 type.[2]

2.2.3.1 Problem -- At the multiphase-actuated intersection controller location, it is desired to skip a particular phase in the event a priority vehicle such as a bus is present at another phase.

The normal phasing of the controller is shown in Figure 9.

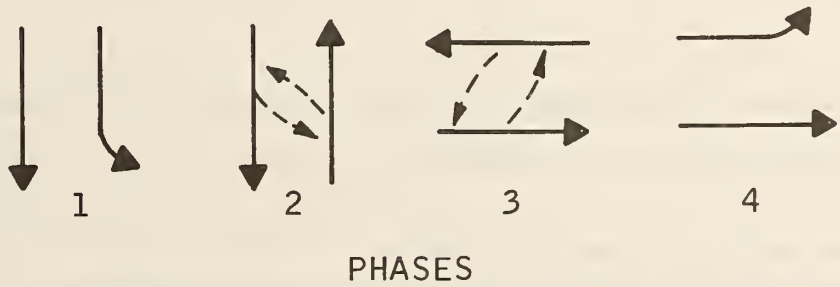


Figure 9. Situation 3 Street/Phasing Diagram

[2]National Electrical Manufacturers Association, NEMA Traffic Control Systems, Standards Publication/No. TS1-1976, 155 East 44th Street, New York, NY 10017.

If a priority vehicle arrives on the phase 2 approach, it is desired to skip phases 4 and 1, if the controller is in phase 3. Also, the controller is to skip phase 1 if the controller is in phase 4 upon detection of a priority vehicle on the approach to phase 2.

2.2.3.2 Solution -- A bus detector-classifier can be used in conjunction with a commercially available phase-selection device or a set of external logic devices installed in the intersection controller to achieve the desired results.

Unlike the last example, no interval modification would be required with a controller designed to NEMA TS1-76, as all of the required control signals necessary for this type of operation are available on this type of controller design. The Honeywell Type-190 was used in this manner for the field evaluation tests.

Referring to Figure 10, the functional hookup to the controller would be as indicated. Both the bus and other vehicle detections are input to the phase 2 detector circuit to ensure a call to the controller to phase 2 in the presence of a bus.

Upon detection of a bus during any phase but phase 2, the phase selector device would turn on phase omit signals for phases 4 and 1. This would cause one or both of the phases to be omitted except if the controller was in phase 1. Upon the controller servicing phase 2, the phase omits would be turned off and the controller would return to the normal operation.

Incidentally, with microprocessor-based controllers, external phase-selector logic may not be needed, since the preempt strategy can be implemented in the controller software.

2.2.3.3 Option 1 -- If it is desired to extend phase 1 for a bus arriving near the end of the phase, the phase 2 "Hold" signal can be made to turn on for

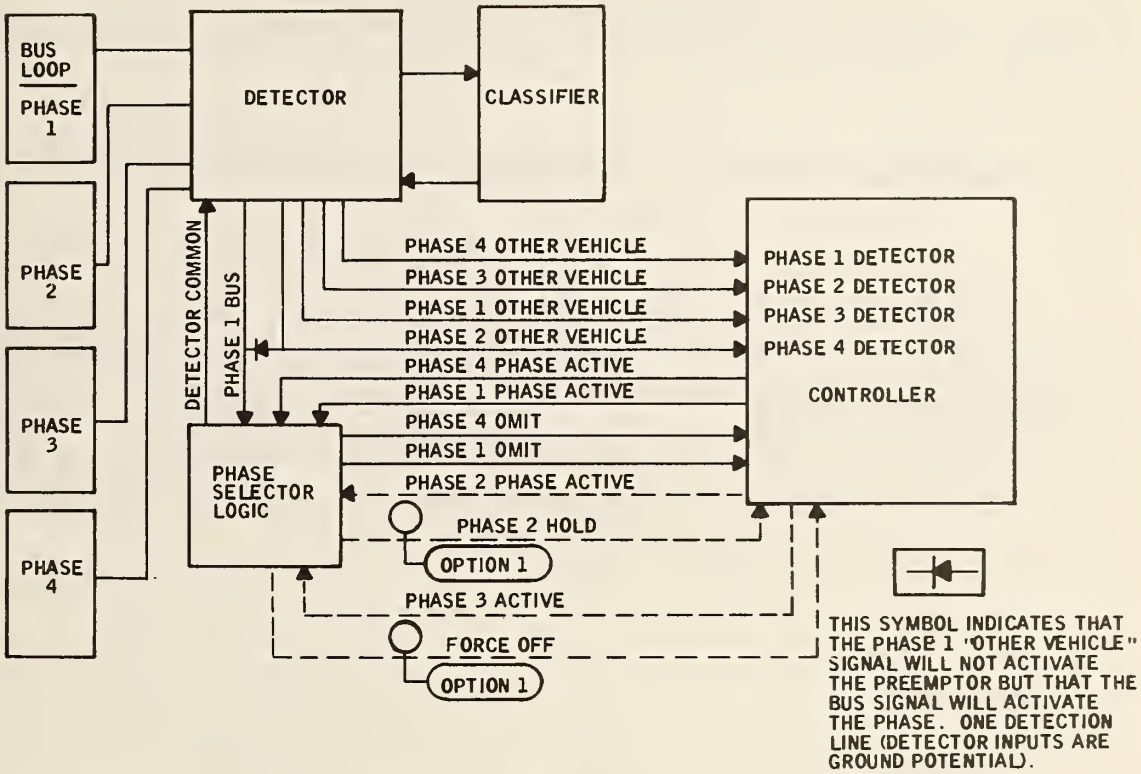


Figure 10. Solution 3 Hookup Block Diagram

the duration of the presence of a bus or for a preset time period upon detection of the bus. This will cause phase 2 to be extended for the late arriving bus.

2.2.2.4 Option 2 -- If it is desired to cause phase 3 to terminate early upon detection of the bus approaching on phase 2, the controller force-off can be activated by the presence of the bus and the phase 3 active signal at the phase-selector logic.

2.2.4 Situation 4

A central computer is selected to do all preempt strategy via communication links.

2.2.4.1 Problem -- Any of the aforementioned examples apply to this situation.

2.2.4.2 Solution -- The outputs of the PBD go directly to the communication link (modem). The central computer takes this information and sends the modified control strategy back to the intersection (controller). The controller operation is modified with a coordination unit either by stopping the dial as in Example 2 above or by stopping the cam. (The traffic engineer can choose the most advantageous solution.)

2.3 CONCLUSION

The preceding discussion has given some examples of the use of the detector-classifier in some applications.

There are numerous other possible applications which could be variations of those suggested and would not add any additional information by discussion here.

In those applications when the equipment is to work within a coordination system, additional measures should be considered in returning the affected controller to coordinated operation after it had serviced the priority vehicle. The method to achieve this will depend on the type of coordination system being used and the type of intersection control.

SECTION 3
INSTALLATION AND OPERATION

3.1 INSTALLATION

3.1.1 Inductive-Loop Transducer

Although the loop and lead-in installation is not extremely critical, some important points should be noted. These considerations will increase the long-term reliability of the installation and maximize the probability of correct classification. They concern:

- Loop wire
- Lead-in wire
- Loop/lead-in splice

A No. 14-gauge stranded wire with Type TW, RHW, XHHW, or THWN insulation should be used for the loop. Wire with PVC (polyvinyl chloride) insulation should not be used because of its poor temperature coefficient. Normal precautions and procedures should be used for making roadway saw cuts so as not to damage the wire.

For lead-in lengths less than 250 ft;* Belden 8720 (No. 14 gauge) wire is recommended. For runs greater than 250 ft;* Belden 8718 (No. 12 gauge) is recommended. Other cable could be used if equivalent to Belden 8718 or 8720 (i.e., twisted shielded pair, cross-linked polyethylene insulation). This wire is recommended because of its low temperature coefficient.

Perhaps the weakest part of an inductive-loop installation is the splice between the loop and lead-in. For the PBD system, there should be only one splice. The following paragraph is one recommended splice procedure:

* 1 ft = .3048 m.

Each loop lead and lead-in conductor shall be stripped back and crimped together with one, two, or three loop-detector conductors as required for the particular installation. The two lead-in conductor splices shall be staggered so that they cannot come into contact with each other. See Figure 11. Each crimp splice shall be soldered and insulated. The insulation material shall be standard black electrical tape or black heat-shrinkable electrical tape available from AMP Special Industries, Valley Forge, PA 19482. The lead-in cable outer insulation and shield shall be stripped back sufficiently to ensure that the shield cannot come into contact with either conductor. The entire splice shall be covered with thick-wall, interior-sealant-coated, heat-shrinkable tubing (available from AMP Special Industries, Valley Forge, PA 19482) or equivalent. The tubing shall extend at least 1 inch* over unstripped insulation in both directions before shrinking the tubing. The tubing shall be shrunk with a heat source delivering at least 250°F,* until the tubing sealant protrudes out both ends of the tubing and is apparent completely surrounding both the lead-in cable and the loop ends. *(1 in. = 2.54 cm. , 250° F = 121° C)

3.1.2 Inductor-Loop Detector Unit

Installing a loop detector for the PBD consists of two steps: 1) tuning the detector to the loop, and 2) setting the detector sensitivity. Tuning is done with controls on each detector and with the Detector Monitor and Select switch on the ILDU power supply section. Detector numbering starts with 1 on the left side and increases to 4 on the right side. See Figure 12.

3.1.2.1 Procedure for Tuning Loop Electronics to Loop and Lead-In -- The sequence for tuning the loop electronics to the loop and lead-in is as follows:

1) If loop lead-in is greater than 190 ft (57.9 m), set jumper (Figure 13) on loop electronics board to connect E1 and E3. If less than 190 ft (57.9 m), set jumper to connect E1 and E2.

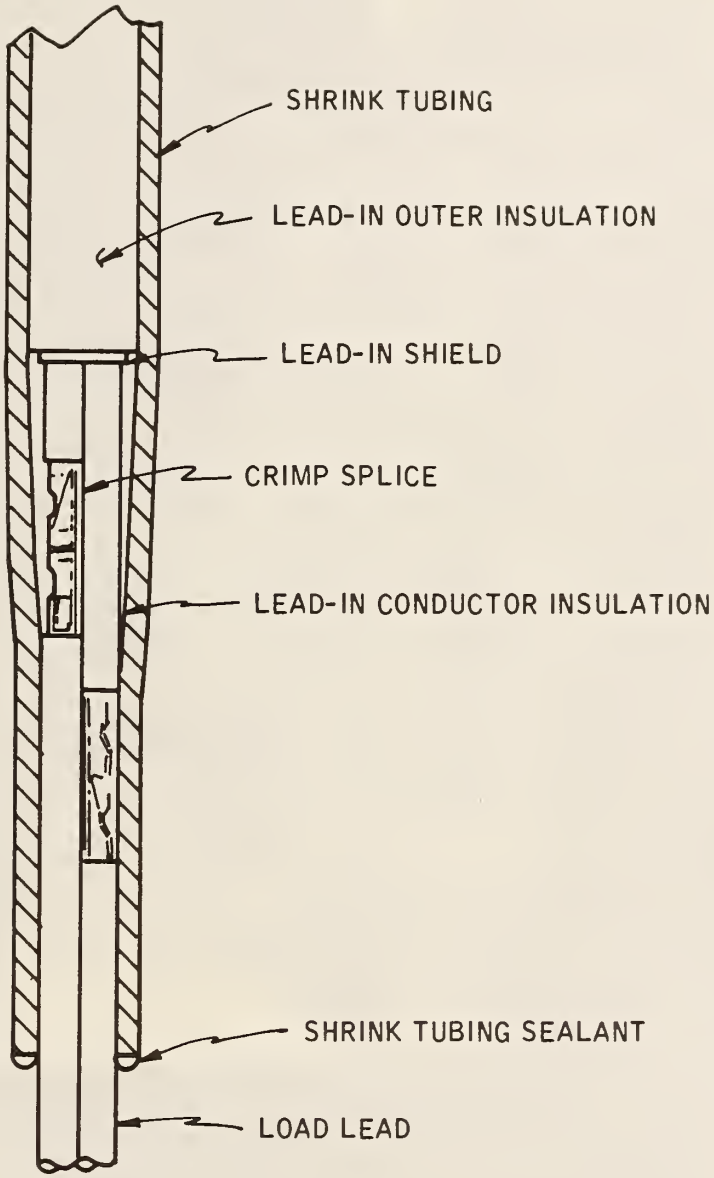


Figure 11. Loop Splice

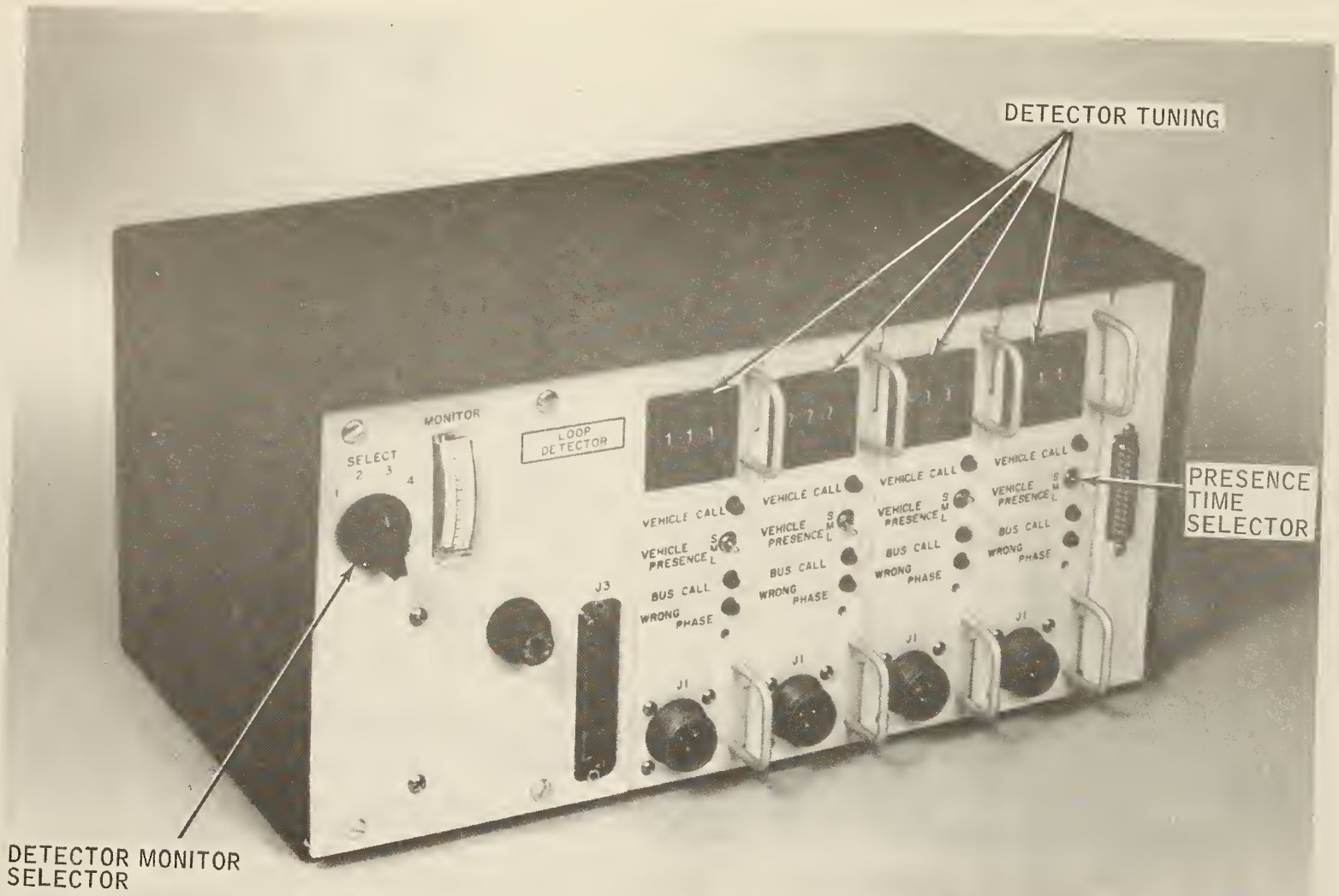


Figure 12. Inductive-Loop Detector (ILD) Controls

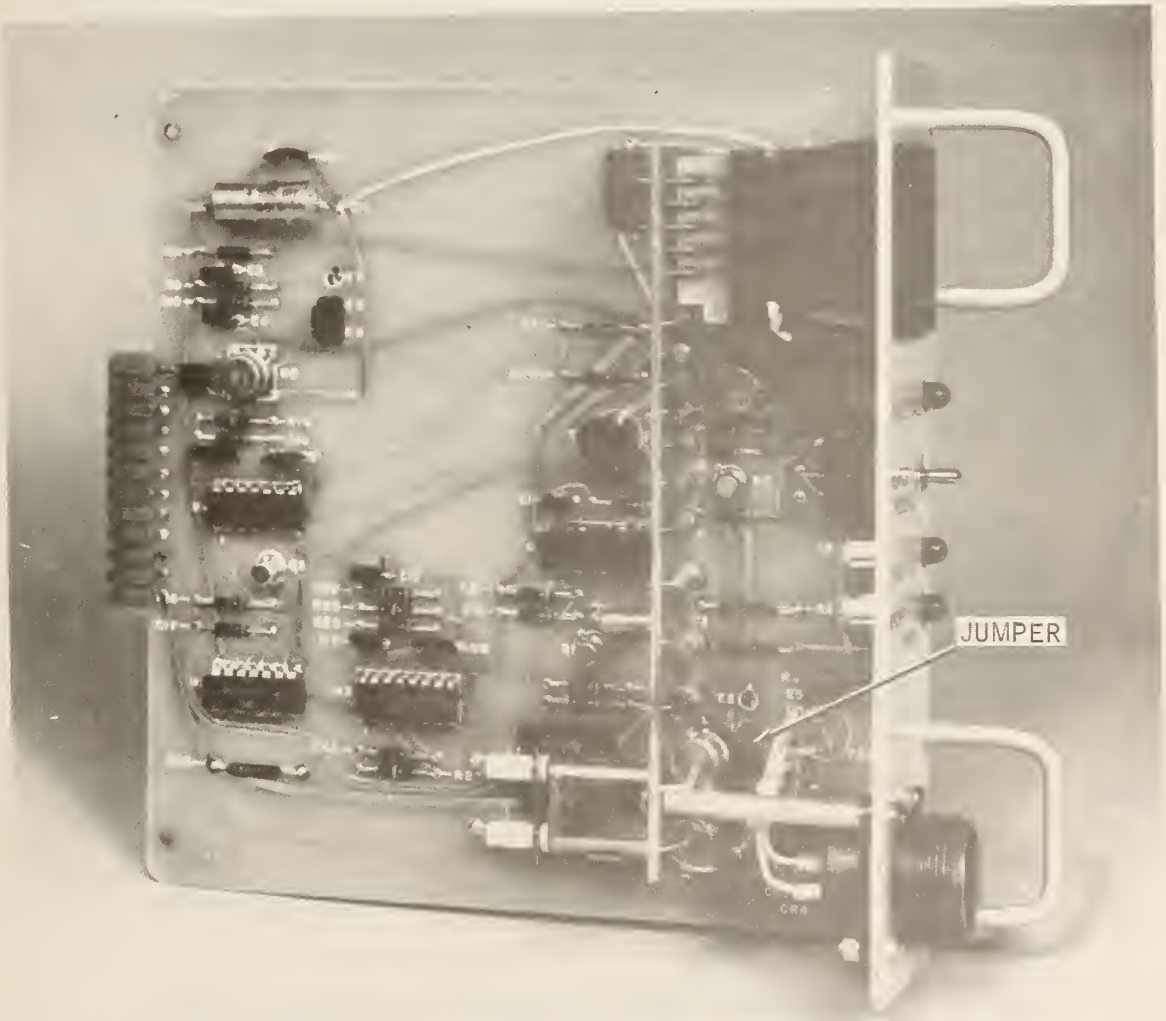


Figure 13. E1/E2/E3 Jumper

2) Select desired detector number on Detector Select switch.

3) Turn sensitivity control maximum clockwise.

4) Set the three capacitor tuning switches to 0. (Coarse tuning light should be off.)

5) Increase setting on left-hand switch until coarse light goes on. Decrease one position.

6) Increase setting on middle switch until coarse light goes on. Decrease one position.

7) Increase right-hand switch until coarse light goes on or monitor meter indicates a minimum voltage.

8) Find present ambient temperature and loop lead-in length on appropriate chart (Figures 14 and 15) to determine compensation factor.

9) Subtract compensation factor from thumbwheel switch setting in Step 6 above.

10) Dial-in the compensated number.

Notes:

- Be sure there are no vehicles over the loop when switch positions are changed.
- The switchover point for capacitor range setting (190 ft) (57.9 m) is for the loop installed in nonreinforced pavement, and loop drive frequency = 100 kHz.
- In reinforced pavement, the switchover point (at 100 kHz) should be approximately 150 ft (45.7 m).

3.1.2.2 Sensitivity Adjustment -- The procedure for adjusting the detector sensitivity is more simple than tuning. This is done with the front panel

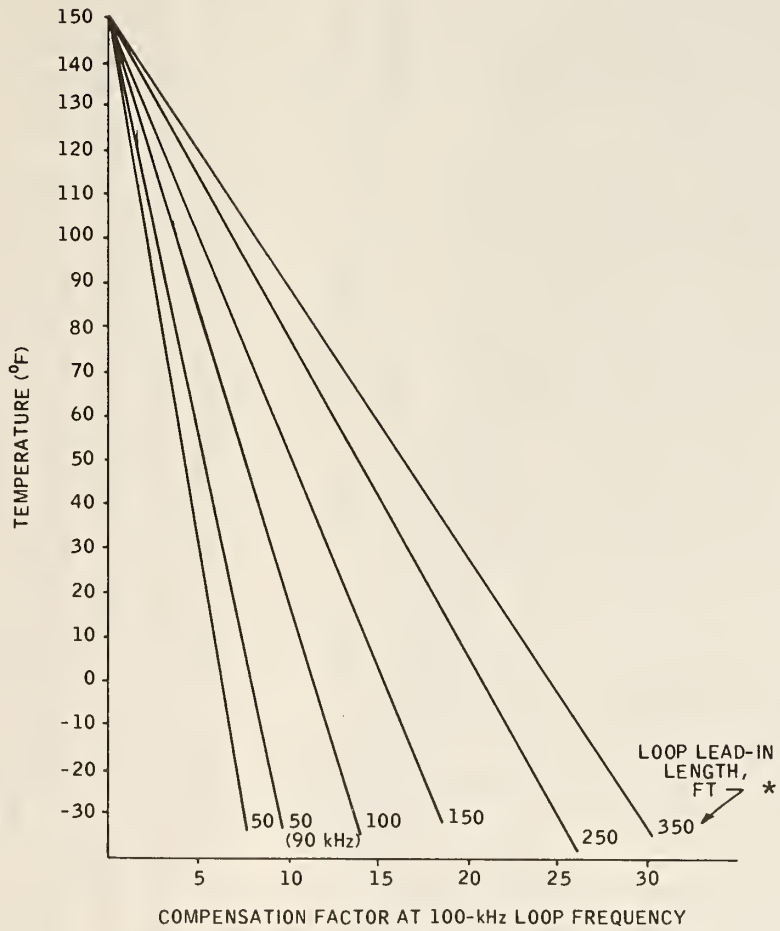


Figure 14. Tuning Compensation -- Nonreinforced Roadway

* 1 ft. = .3048 m.

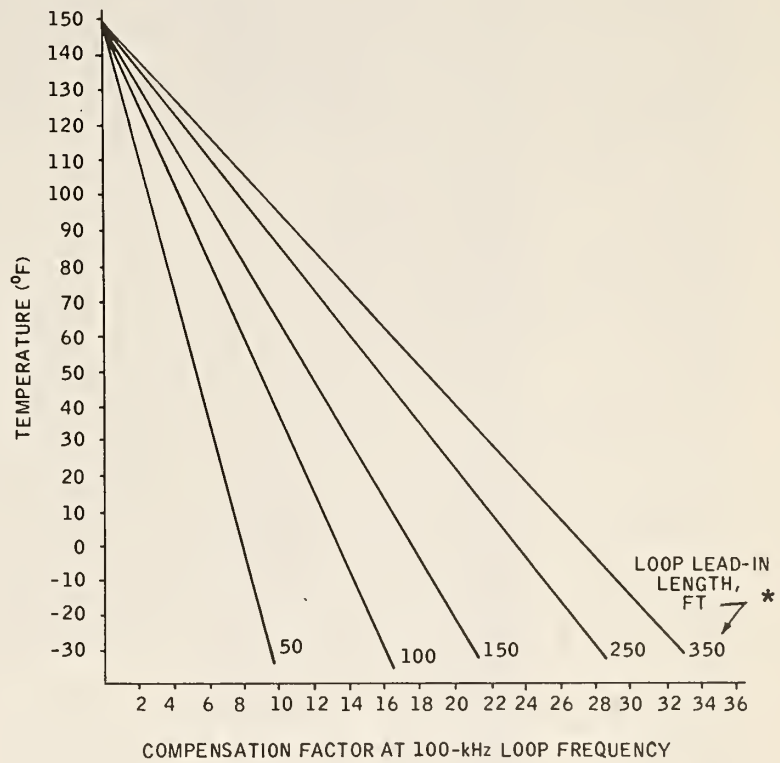


Figure 15. Tuning Compensation -- Reinforced Roadway

control, jumpers E6, E7, and E8, and the Monitor meter. Jumpers for this function are located on the electronics board (Figure 16) and should be positioned according to Table 1. Next, select the desired detector number on the Detector Select switch. Turn the sensitivity control fully counter-clockwise. While observing the Monitor meter, slowly increase the sensitivity until the following conditions are met:

a) Vehicles produce outputs from 2 to 3V to 10V (vehicles with lower ground clearance produce higher outputs).

b) Mass-transit buses should have a minimum peak output of 3V, and a maximum of 9V, total.

Table 1. Jumper Settings

Loop Lead-In Length		Jumper Position	
Feet	Meters	Reinforced Roadway	Nonreinforced Roadway
0 to 90	0 to 27	E6 - E8	E6 - E8
90 to 440	27 to 134	E6 - E7	E6 - E8

3.1.3 Bus Classifier Unit

In most installations, no adjustments to the BCU will be necessary at installation time. The E-switch and T-switch located on preprocessor card No. 1 and shown in Figure 17 are the only items in the BCU that are field-adjustable.

3.1.3.1 E-Switch -- This switch governs the sensitivity of the digital peak detector (see Section 4, Theory of Operation). The switch generates a binary number, with the least-significant bit (LSB) on the right (Figure 17, location 11C). A smaller binary number increases the peak detector sensitivity, and vice versa. The switch is factory-set to 5.

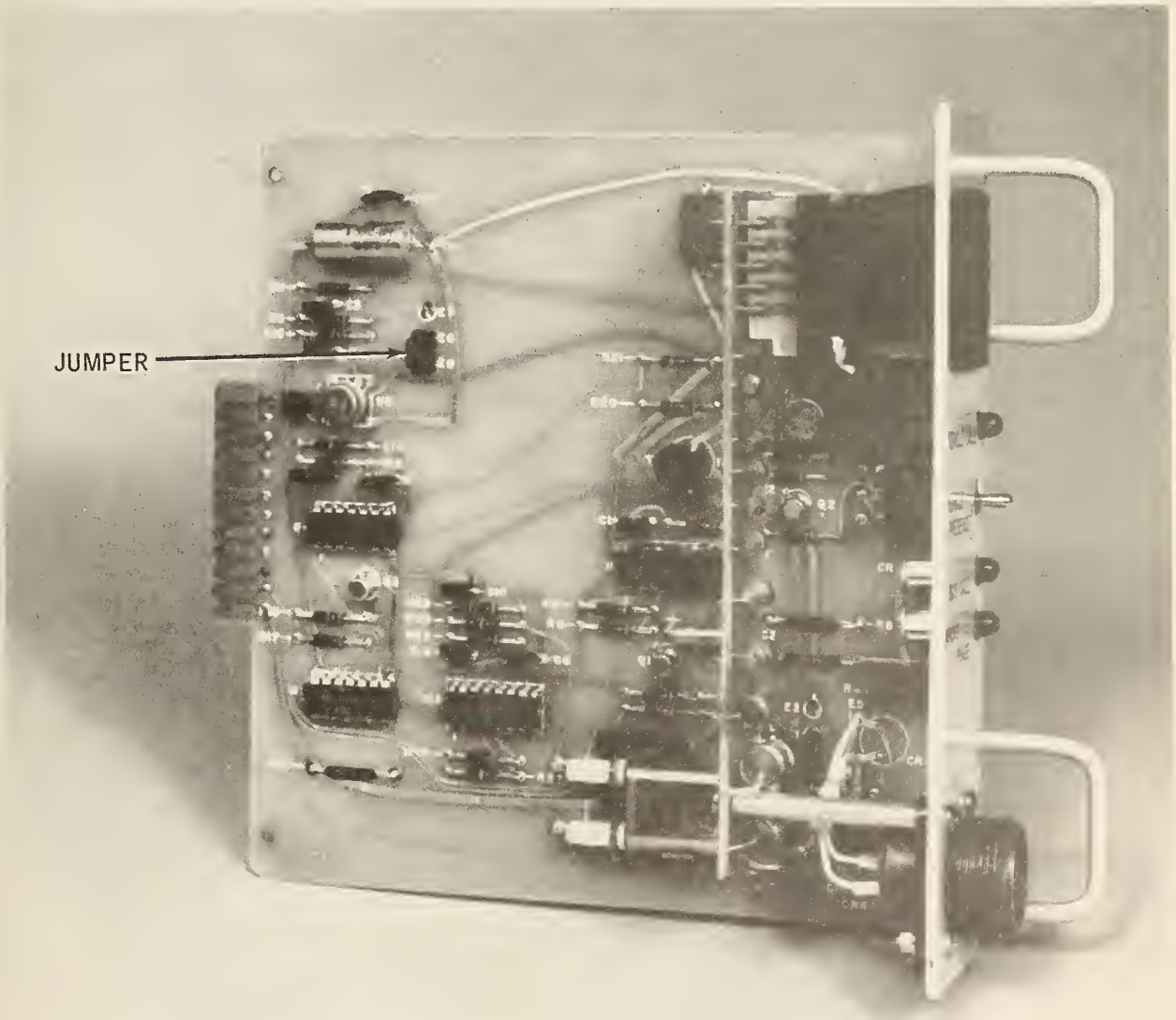


Figure 16. E6/E7/E8 Jumper

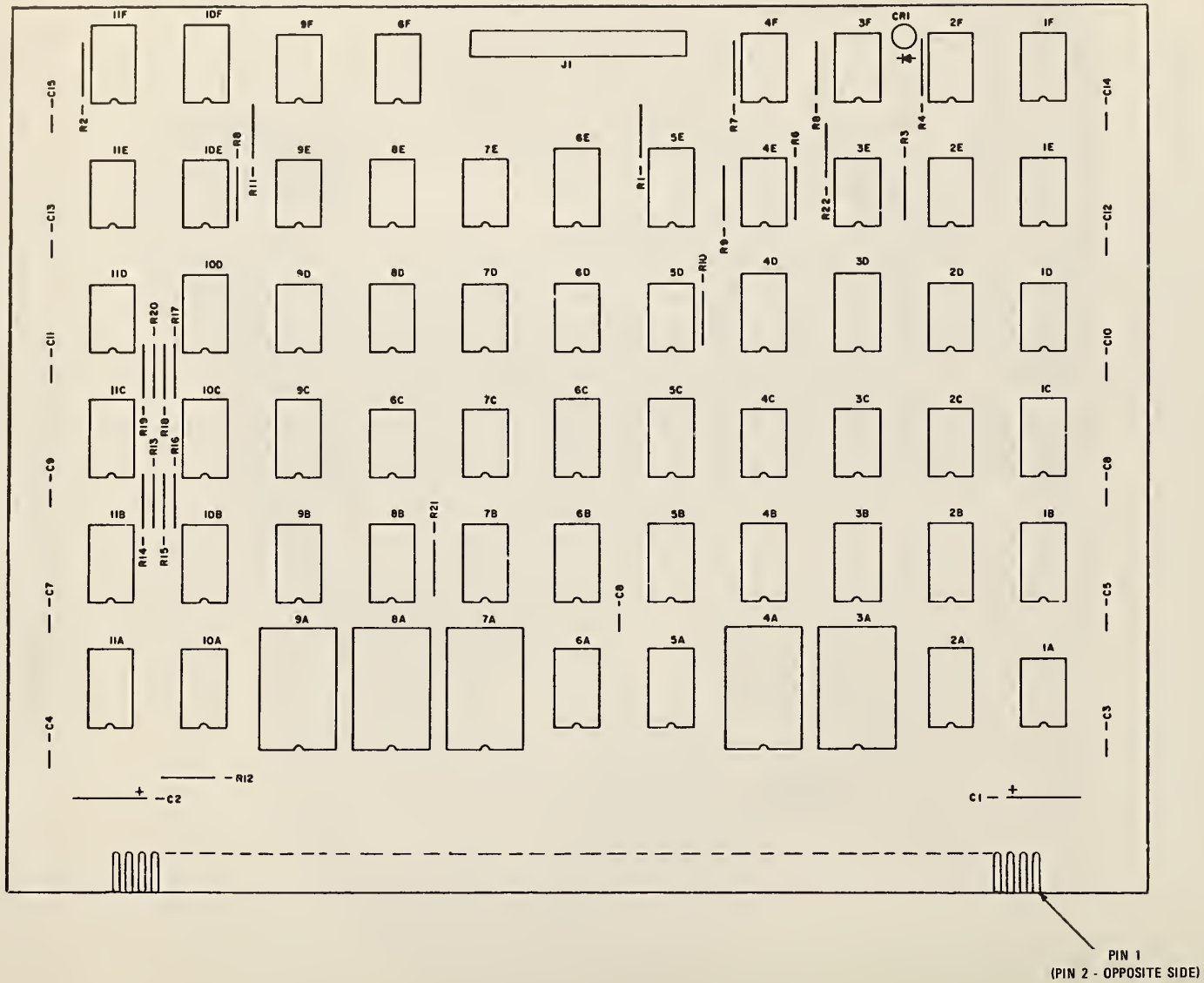


Figure 17. BCU E- and T-Switches (Preprocessor Module)

3.1.3.2 T-Switch -- This switch sets a voltage above the background (long-term average) value where the beginning and end of vehicle signatures are sensed. (See Section 4, Theory of Operation.) The switch generates a binary number, with the LSB on the right (Figure 17, location 11B). A smaller binary number decreases the threshold, and vice versa. The switch is factory-set to 6.

3.2 OPERATION

3.2.1 Retuning the ILD

If at any time it is necessary to retune a detector, the procedure in 3.1.2.2 should be followed. After this is done, the System Clear switch on the BCU should be pressed and released. Failure to do so may prevent vehicle detection and bus classification on that detector.

3.2.2 System Clear

After the installation procedures in 3.1 are completed or it is desired to restart the PBD system, the System Clear switch should be pressed and released.

3.2.3 Test Request

In addition to the background diagnostic tests done in the BCU, an additional test is available to the operator. When the Test Request switch is pressed and held, the following should occur: 1) All vehicle call and bus call lights on the ILDU should light. 2) All vehicle and bus call relays should energize. 3) When the switch is released, all lights and relays should return to normal

If this test is failed, the diagnostic procedures in Section 5, should be consulted.

3.2.4 General

Once the installation procedures are implemented and the System Clear switch on the BCU has been pressed and released, the PBD may be monitored for proper operation. If a vehicle was on a loop at the time the System Clear switch was exercised, several seconds may elapse before proper bus classification will occur. Otherwise, after 5 seconds or less, the PBD system should be operating properly. This can be observed by watching the ILDU vehicle and bus call lights in conjunction with vehicular traffic over the corresponding loop.

Any time any vehicle enters the loop, a vehicle call should occur for that detector. If long-vehicle presence has been selected, the call should remain on until vehicle passage. Within 0.2 second after bus passage, the bus call light should remain on for 0.5 second.

SECTION 4
THEORY OF OPERATION

The PBD system consisting of a BCU and one to four ILDUs has a simple system structure. The BCU acts as a supporting subsystem to the ILDUs. However, to the traffic engineer and to control systems in the intersection cabinet, the PBD system merely appears as "smart" ILDs. This is because all PBD interfacing with other systems, such as the traffic controller, is done through the ILDs. Figure 18, shows this relationship more clearly. The loops from the roadway go the ILD and, as a result, the bus/no-bus decision comes from the relays in the ILD.

The discussion of the theory of operation of the PBD system will be broken into these two subsystems. Each subsystem will be treated as an entity but can be related back to Figure 18.

4.1 INDUCTIVE-LOOP DETECTOR UNIT

The ILDU consists of a power supply and chassis with one to four ILDs (Figure 19); the power supply is shared.

4.1.1 Power Supply

Power supply operation is discussed with reference to its schematic (Drwg. No. 10059902, see Section 7).

The power supply delivers two voltages for the ILDU. Unregulated 25 Vdc is supplied for use by the vehicle and bus call relays (R11 et al.) and all light-emitting diodes (LEDs). Transformer T1 and power rectifier diodes

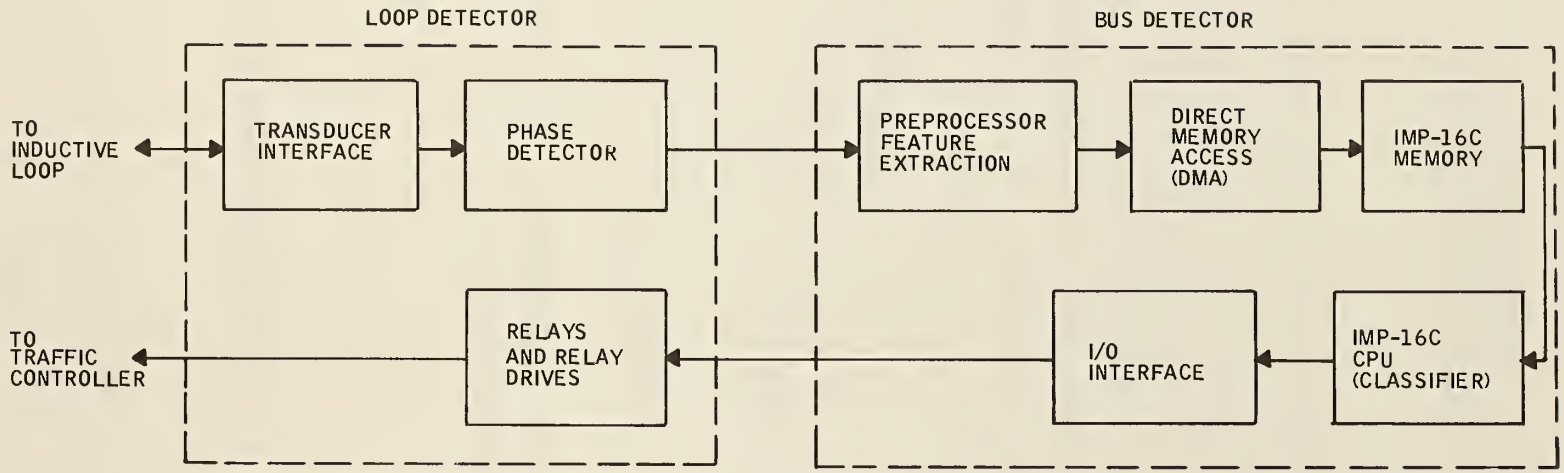


Figure 18. PBD Data Flow

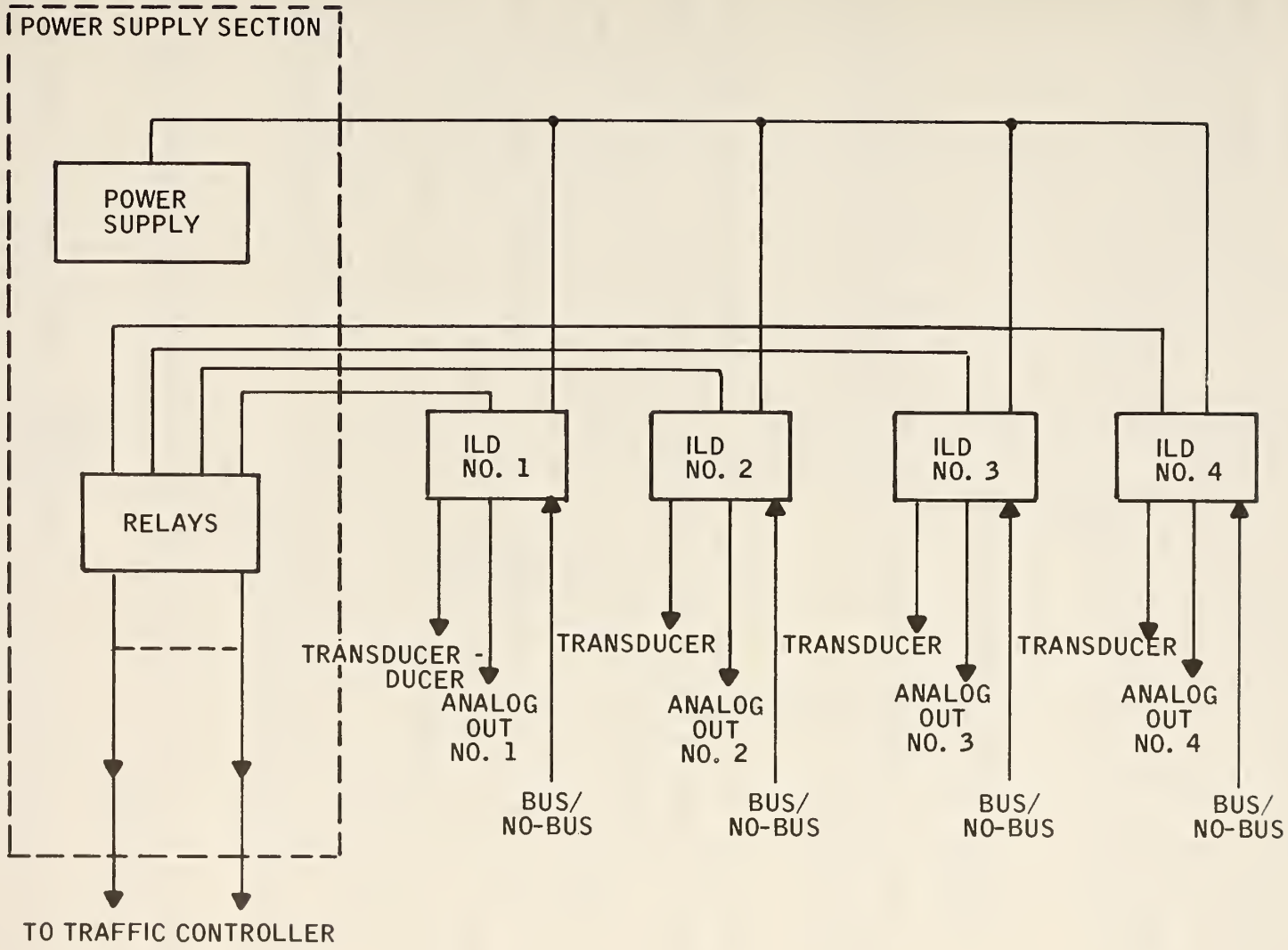


Figure 19. ILDU Functional Block Diagram

CR10 and CR11 supply a nominal 25 Vdc (115 Vac input). Monolithic voltage regulator U1, in conjunction with pass transistor Q9, supplies regulated 12 Vdc ± 0.5% for use by the ILD electronics. Q1, CR1, and R1 constitute the typical relay driver circuit. U2 is a buffer amplifier for meter M1. Switch S1 selects the desired ILD output to be monitored.

4.1.2 Inductive-Loop Detector

ILD operation is discussed with reference to its schematic (Drwg. No. 10059903, see Section 7). Figure 20 is a block diagram of the ILD loop transducer circuits.

A crystal oscillator, U3, operating at $2f_o$, is divided by two by flip-flop U2. Flip-flop U2 supplies a reference signal to phase detector U4 and the loop driver U3. Thumbwheel switches S1, S2, and S3 select the appropriate tuning capacitors, C1 through C12, for loop resonance. Jumper J1 provides additional capacitance for short loop lead-ins. The circuit consisting of R23, R24, CR5, CR4, and DS1 is used to suppress high-voltage transients (lightning, etc.) which might appear at the loop inputs. Transformer T1 takes the common mode signal off the loop to the zero-crossing detector, U6. The loop signal is further shaped by U4 and sent to the phase detector, U4, and flip-flop U2. The output of the phase detector is integrated by network R13, R14, and C5 and amplified by U5. Jumper J2 selects a high/low sensitivity range for the ILD.

Flip-flop U4 is used to determine when the phase-detector output is on the wrong side of null.

Monostable multivibrators, U1, in conjunction with switch S4, determine the length of time the vehicle call relay is energized (short, medium, long).

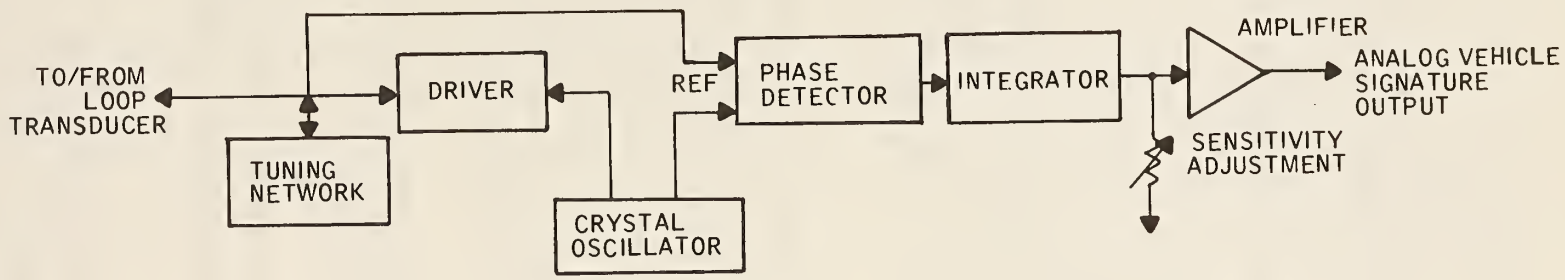


Figure 20. ILD Block Diagram

4.2 BUS CLASSIFIER UNIT

The BCU is organized around the National Semiconductor IMP-16 microcomputer. A block diagram of the operational structure (Figure 21) shows the bus-oriented nature of the BCU. The BCU is an interrupt-driven system. Figure 22 shows the order of card locations in the chassis.

4.2.1 Input/Output Module

I/O module operation is discussed with reference to the I/O schematic (Drwg. No. 10059899, see Section 7). Three functions are performed on this card: system auto-restart, real-time clock, and ILD relay driver interface.

The auto-restart circuit monitors the +5V supply for low voltage via comparator 4C and R23. When low voltage is detected, 4C trips flip-flop gate 6C. Recovery time is governed by CR2, R13, and C14. The output of the auto-restart circuit is "OR"ed with the System Clear switch, S1, and goes to other BCU cards. Auto-restart can also be initiated by the central processor unit (CPU) via flag 13 and monostable multivibrator 6D. CPU-generated auto-restart can be inhibited by switch S3.

Flip-flop 8D (left half) monitors the occurrence of a CPU-initiated auto-restart and drives fault 2 indicator.

Flip-flop 8D (right half) monitors the occurrence of a CPU-diagnosed random-accessed memory (RAM) error via flag 11 and drives fault 1 indicator.

A 0.2-second-period real-time clock for the BCU is made of gated stable multivibrator 7A and flip-flop 9A. Flip-flop 9A drives the CPU general interrupt line until it is cleared by the CPU via 9B or stopped by the CPU via 10B.

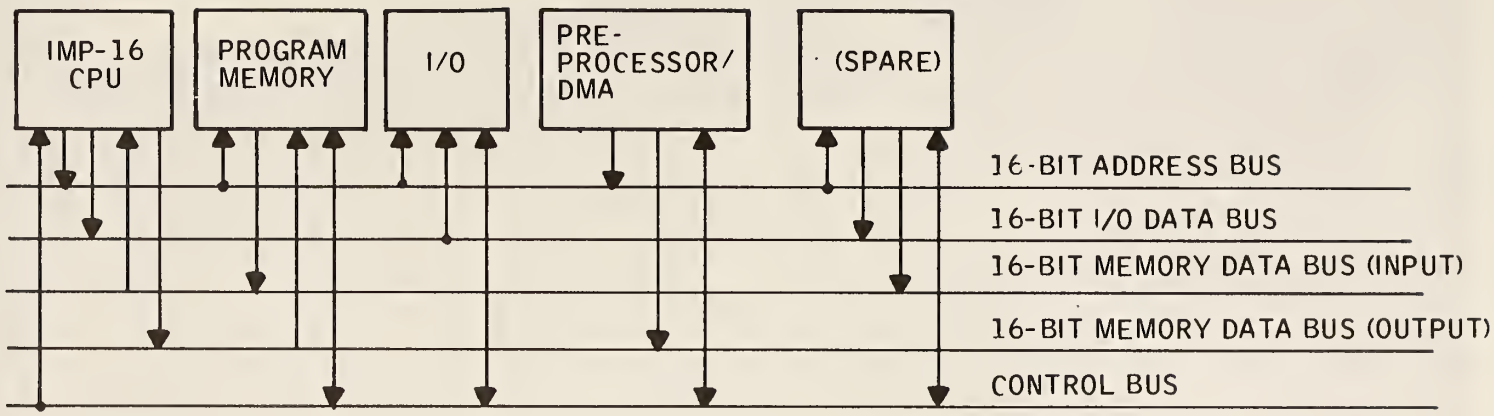


Figure 21. IMP-16 Bus Structure

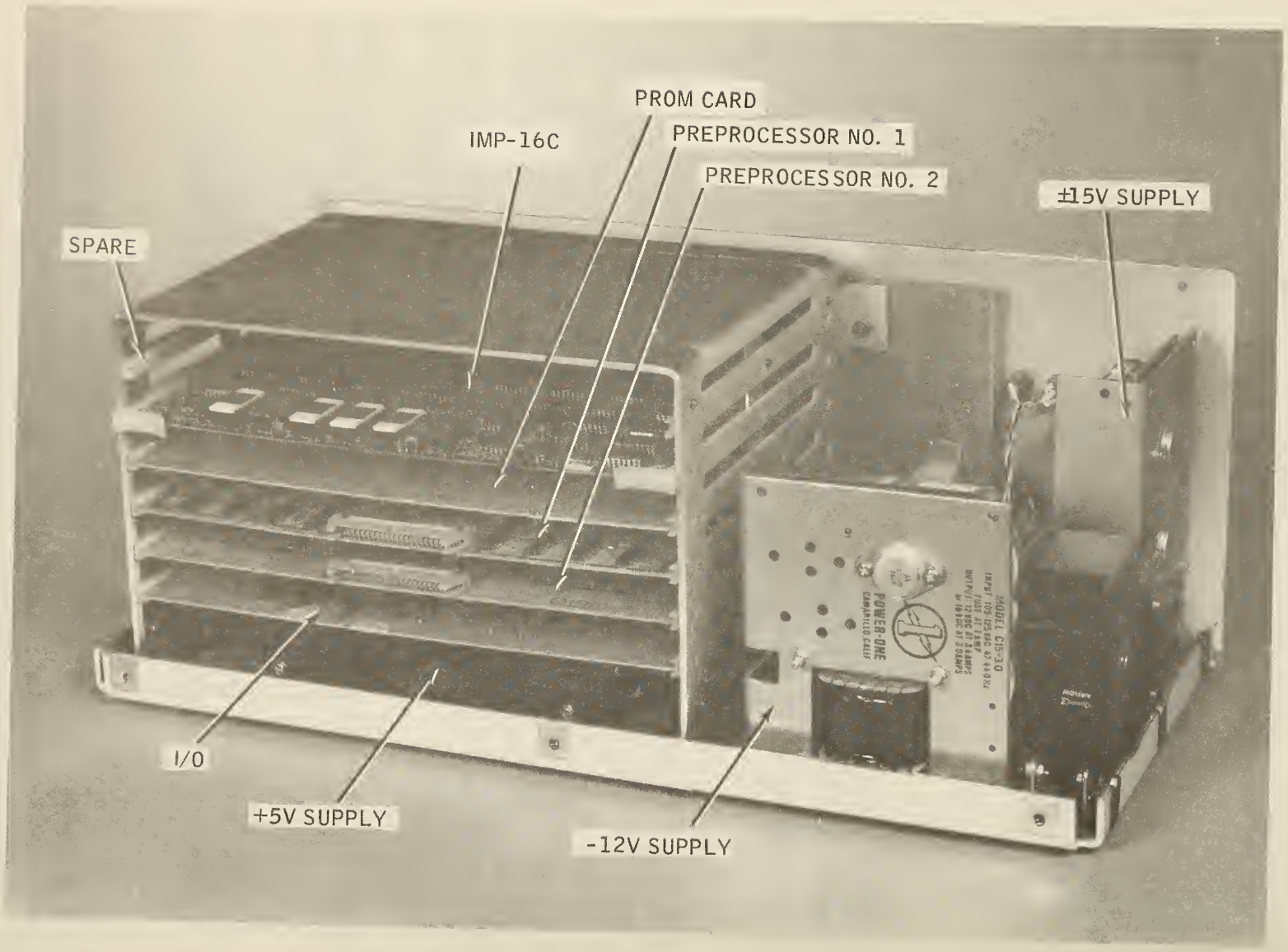


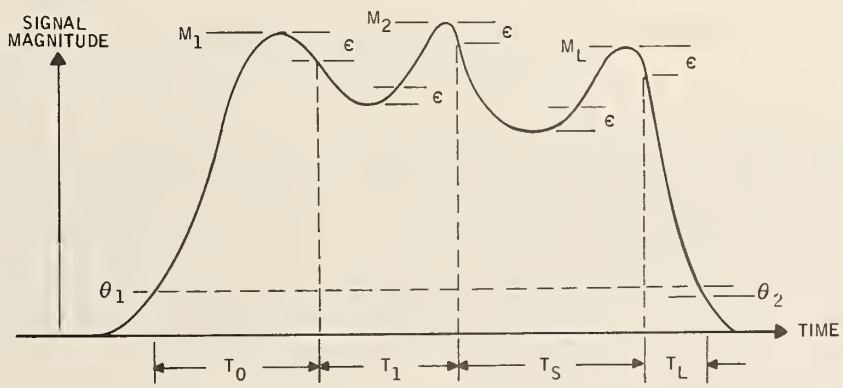
Figure 22. Card Designations (Rear View)

Hex flip-flops 2B through 5B are the latches for bus/vehicle output for each ILD. 1A through 5A are open-collector buffers.

Circuits 8B, 8C, and 9C are address decoders which decipher what function is to be performed on the I/O card. Debounce flip-flop 8B with switch S1 is a CPU jump condition input for diagnostic purposes. Debounce flip-flop 10A and switch S2 form the test request circuit located on the BCU front panel.

4.2.2 Preprocessor Module

The primary purpose of the preprocessor is to extract the important features from each loop detector signal, up to a maximum of 16 ILDs, and store these features in the IMP-16 memory. Figure 23 is a sketch of an idealized bus signature showing the primary signature features extracted. These features are the values of the signature peaks and their associated time intervals. The secondary function of the preprocessor is to determine vehicle presence. Presence information is sent to the IMP-16 memory for processing.



PRIMARY FEATURES

T_0 = TIME FROM TURN-ON TO FIRST PEAK

T_1 = TIME FROM FIRST PEAK TO SECOND PEAK

T_S = TIME FROM SECOND PEAK TO LAST PEAK

T_L = TIME FROM LAST PEAK TO TURN-OFF

M_1 = MAGNITUDE OF FIRST PEAK

M_2 = MAGNITUDE OF SECOND PEAK

M_L = MAGNITUDE OF LAST PEAK

Figure 23. Bus Signature Primary Features

The preprocessor consists of two printed-circuit cards. These cards contain the analog interface to the loop detectors (ILDs) and the direct-memory address (DMA) interface to the IMP-16 RAM, among other functions. Figure 24 is a block diagram of the preprocessor showing the gross partitioning of the functions on each card.

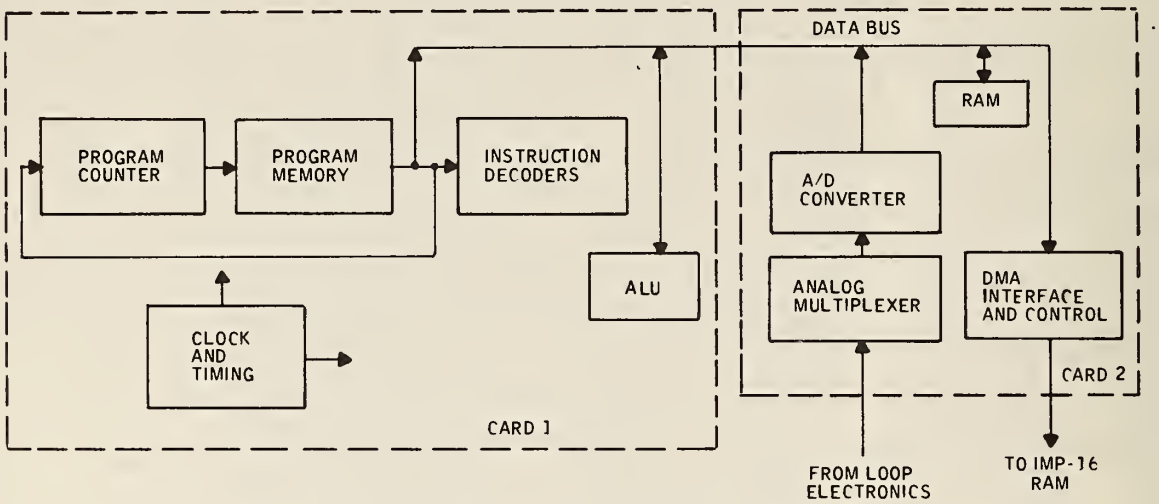


Figure 24. Preprocessor Block Diagram

Card 1 is represented by schematic diagram 10059904 (see Section 7). On sheet 1, 3C and 4C comprise the program counter which feeds a latch, 3D and 4D. The preprocessor program is contained in programmable read-only memories (PROMs), 2B, 3B, and 4B. 2A, 3A, and 4A decode the program instructions and control the individual registers, memory, etc., in the remainder of the preprocessor. 1C and 1B, with associated circuitry, generate the preprocessor clocks which control the timing of the preprocessor. 5E, 6E, and associated circuitry, generate and control the 250-μs interrupt for polling of the detectors.

Sheet 2 shows the arithmetic logic units (ALUs), 7A, 8A, and 9A, and associated support registers, 6A, 10A, 5A, 11A, 7B, 8B, and 9B. 6B and 10B comprise a general-purpose register used for temporary data storage. 6C and 9C are additional instruction decoders for preprocessor control. 10F is

a flag register and feeds 11F, the jump multiplexer. 10C, 5C, 11B, 5B, and 11C are tristate data buffers. The T-switch sets the threshold voltage (above background) at which vehicle presence is detected (θ_1 of Figure 23). The E-switch selects the sensitivity of the peak detector routine (ϵ of Figure 23).

Card 2 is represented by schematic 10059901 (see Section 7). On sheet 1, the DMA interface control is shown. 11D latches a DMA request under program control. When the IMP-16C is not using memory, 9B enables shift register 10D, which generates the timing signals for the DMA cycle. 9B (right half) controls the data and address bus drivers located on sheet 2.

Sheet 2 shows the 16-channel analog multiplexer, 4A, and A/D converter, 2C. 3B and 4C are tristate data buffers. 4B and 7C comprise the RAM address register for RAM 5D, 6D, and 7D. The DMA address register is 5B and 8B, with bus drivers 7A, 8A, and 10C. The DMA data register is 2B and 6B with bus drivers 6A, 2A, and 5A.

4.2.3 Programmable Read-Only Memory Module

PROM operation is discussed with reference to its schematic (Drwg. 1005990, see Section 7). This card contains all PROM for the IMP-16 CPU. Memory chips 1C through 10C are erasable PROMs. 4A and 5A are address buffers. 6A and 8B are address decoders which select the memory chip pair in which the desired data are located. 1A, 2A, and 3A are tristatable memory output data buffers.

Circuits 7A, 8A, and 9A are buffers for the debug card, general interrupt circuit, and the DMA.

4.2.4 Central Processor Unit Module

The theory of operation of the IMP-16C is covered in detail in Section 9 of the IMP-16C Application Manual. This subsection will therefore treat only the general aspects of the IMP-16C.

Figure 25 is a block diagram of the CPU card, showing the major functions on it. These major functions are:

- Central processing unit
- Clock generators
- Input multiplexer
- Data buffer
- Control flags
- Conditional jump multiplexer
- On-Card memory
- Address latches

The CPU is configured around the National Semiconductor GPC/P (general-purpose controller/processor) metal-oxide semiconductor/large-scale integration (MOS/LSI) devices, as shown in the block diagram. The MOS/LSI devices consist of one CROM (control read-only memory) and four RALUs (register and arithmetic logic units). Each RALU handles four bits, and a 16-bit unit is formed by connecting four RALUs in parallel. A 4-bit-wide control bus is used by the CROM to communicate most of the control information to the RALUs. The CPU includes provision for adding a second CROM for an optional extended instruction set which is used in this system.

The clock generator provides the MOS clock drivers and CPU timing signals. The system clock is distributed outside of the IMP-16C for synchronization of peripheral units with the IMP-16C.

External to the MOS/LSI circuits but still within the IMP-16C are control flags for both the IMP-16C and external interfacing circuits. These control flags are in addition to the status flags that are internal to the RALUs.

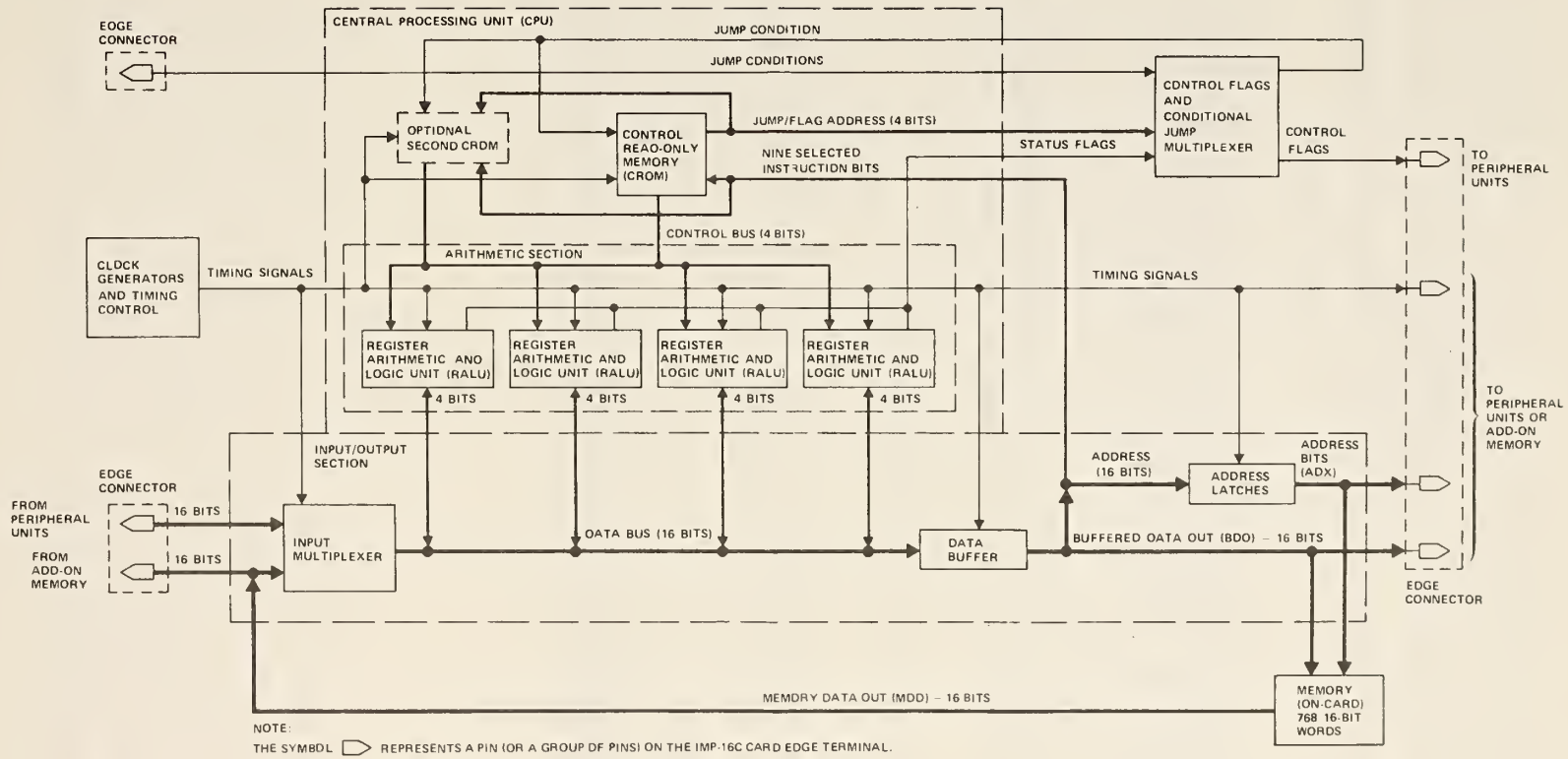


Figure 25. IMP-16C Simplified Block Diagram

The status flags are discussed in the description of the CPU. The control flags are discussed in Section 9 of the IMP-16C Application Manual under Control Flag instructions. Conditional branches are selected by the conditional jump multiplexer. These branch conditions are discussed in the manual under Branch-On-Condition (BOC) instructions.

Data from the user's peripheral devices and add-on memory are received by the input multiplexer. Data from the on-card memory are also processed through the input multiplexer en route to the CPU.

Output data are made available from the 16-bit data buffer via the card-edge connector to the user's peripheral devices and add-on memory. A 16-bit address bus is also brought out to the card-edge connector for addressing both add-on memory and peripheral devices.

The memory on the IMP-16 card consists of 1024 words of read/write memory and sockets for 1024 words of PROM or ROM. A maximum of 65,536 words may be addressed.

The IMP-16C Application Manual is referenced in the Appendix; for a detailed description, see Volume II of this report.

SECTION 5
DIAGNOSTICS

This section provides the necessary information required to maintain the PBD system in proper operating condition. The functional modularity of the PBD system allows rapid diagnosis to printed-circuit card level. Once the defective card has been isolated, the card would be returned to the factory for repair. Also, since there are only a few printed-circuit cards in the system, card substitution is a rapid method of correcting the system malfunction.

Fault-isolation procedures would most likely take place in one of two locations. This would be at the field (i.e., intersection) or at the shop level. The application of these procedures is left to the user's discretion.

Because of the nature of the equipment and the desire to return the intersection to normal operation as soon as possible using a minimum of equipment, the recommended technique used at the field level is essentially one of ILD or BCU module substitution.

5.1 GENERAL

Maintenance personnel shall observe intersection light operation, ILD and BCU status lights, and record such observations for use at the shop level of repair, should that become necessary. Maintenance personnel will have previously determined that an intersection control system problem exists. The procedure contained herein will aid in determining whether or not the PBD system consisting of the ILDU and the BCU are functional.

In general, only two basic symptoms will be evident when the PBD system fails. Either one or more ILDs will fail to tune, or one or more detector channels will fail to classify busses properly. Procedure 1 below addresses misclassification; Procedure 2 below addresses ILD tuning failure.

5.2 DIAGNOSTIC PROCEDURES

Follow Figure 26 from the starting point and replace the appropriate module(s) when a fault is detected. Then restart the test procedure and continue until the problem is resolved. A voltage-ohm-milliammeter (VOM) will be needed for performing voltage and resistance checks.

5.2.1 Procedure 1

The PBD fails to classify properly. Follow Figure 26.

5.2.2 Procedure 2

The ILD fails to tune properly. This procedure (see Figure 27) assumes that the loop connections are properly made with the ILDU.

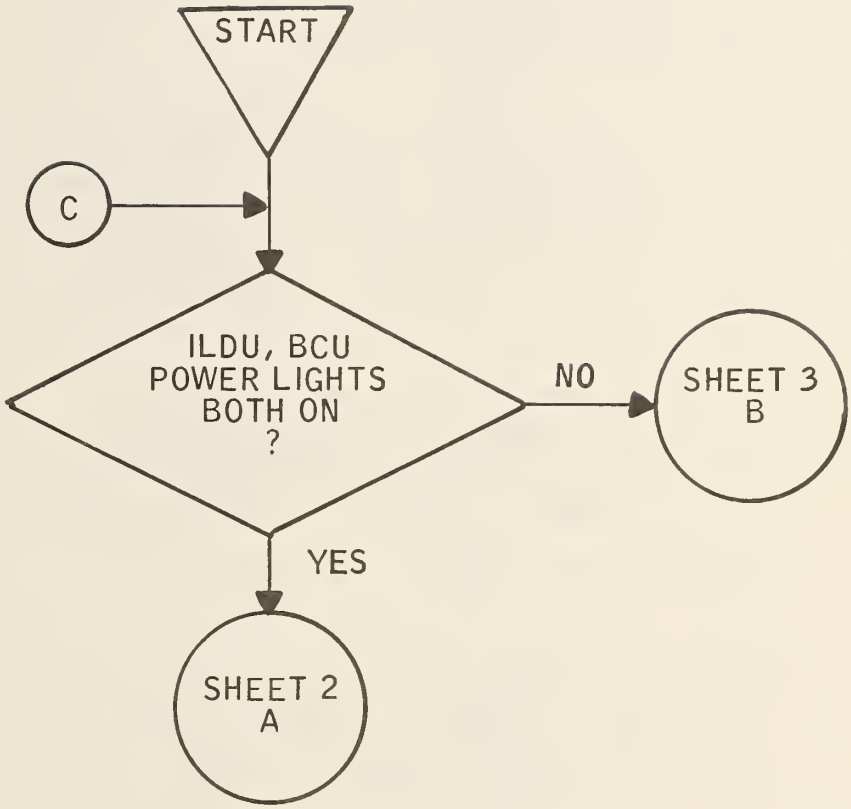
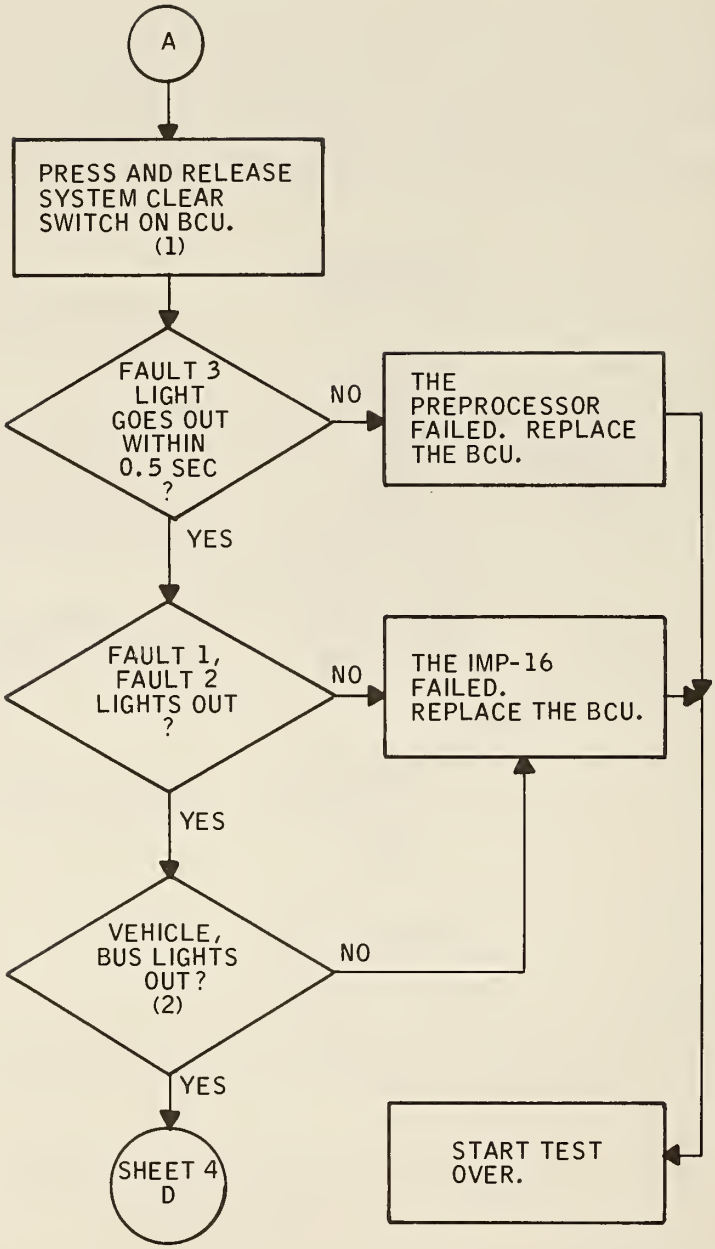


Figure 26. Diagnostic Flow Chart
(Sheet 1 of 11)



NOTES:

(1) IT IS PREFERRED TO DO THIS WHEN NO VEHICLES ARE ON OR NEAR THE STREET LOOPS; THIS ENSURES DESIGNATED STATUS LIGHTS ARE OUT DURING SUBSEQUENT TEST.

(2) IF VEHICLES OR BUSSES ARE NEAR LOOPS, THOSE CORRESPONDING LIGHTS MAY COME ON.

Figure 26. Diagnostic Flow Chart (continued) (Sheet 2 of 11)

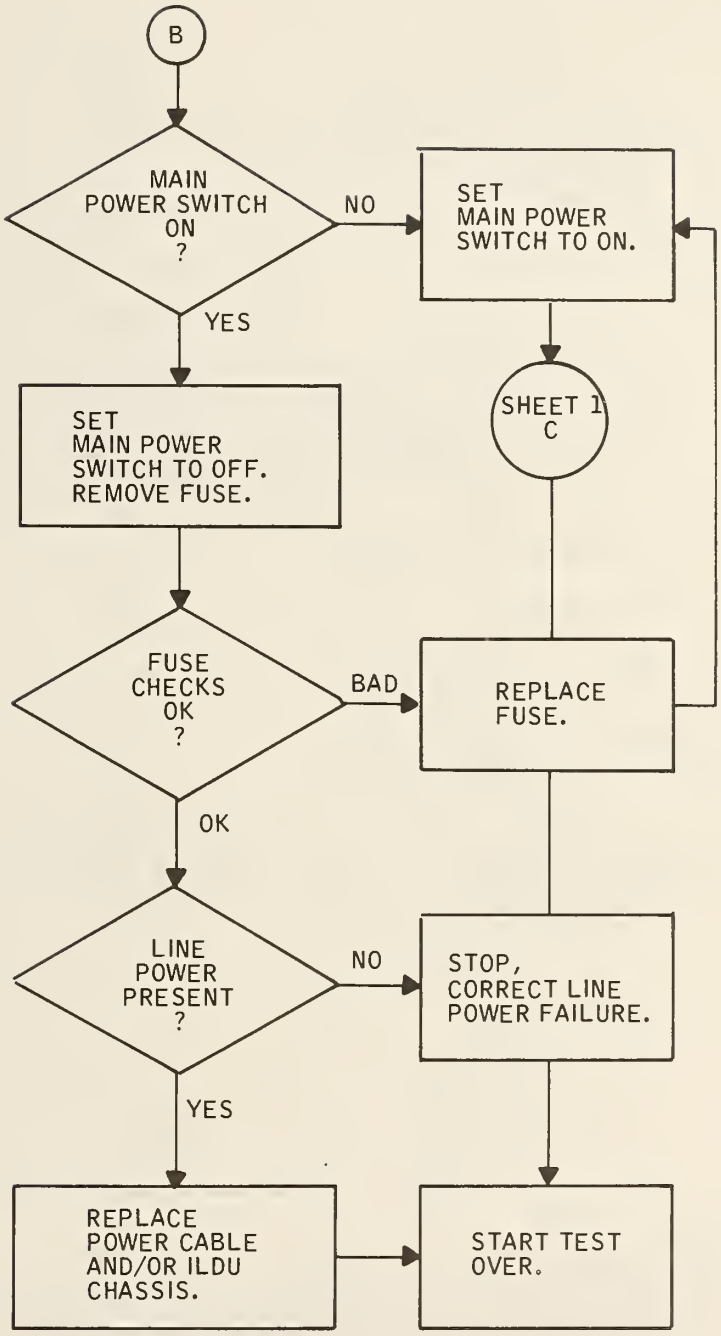
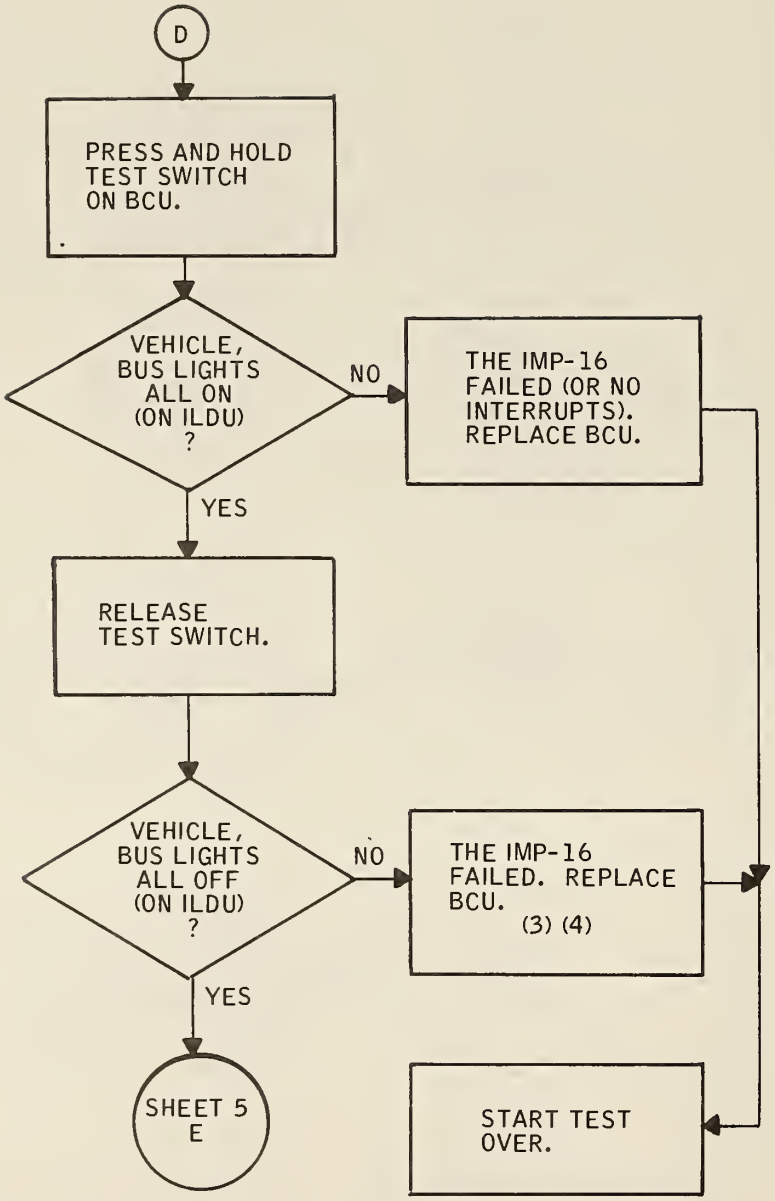


Figure 26. Diagnostic Flow Chart (continued)
(Sheet 3 of 11)

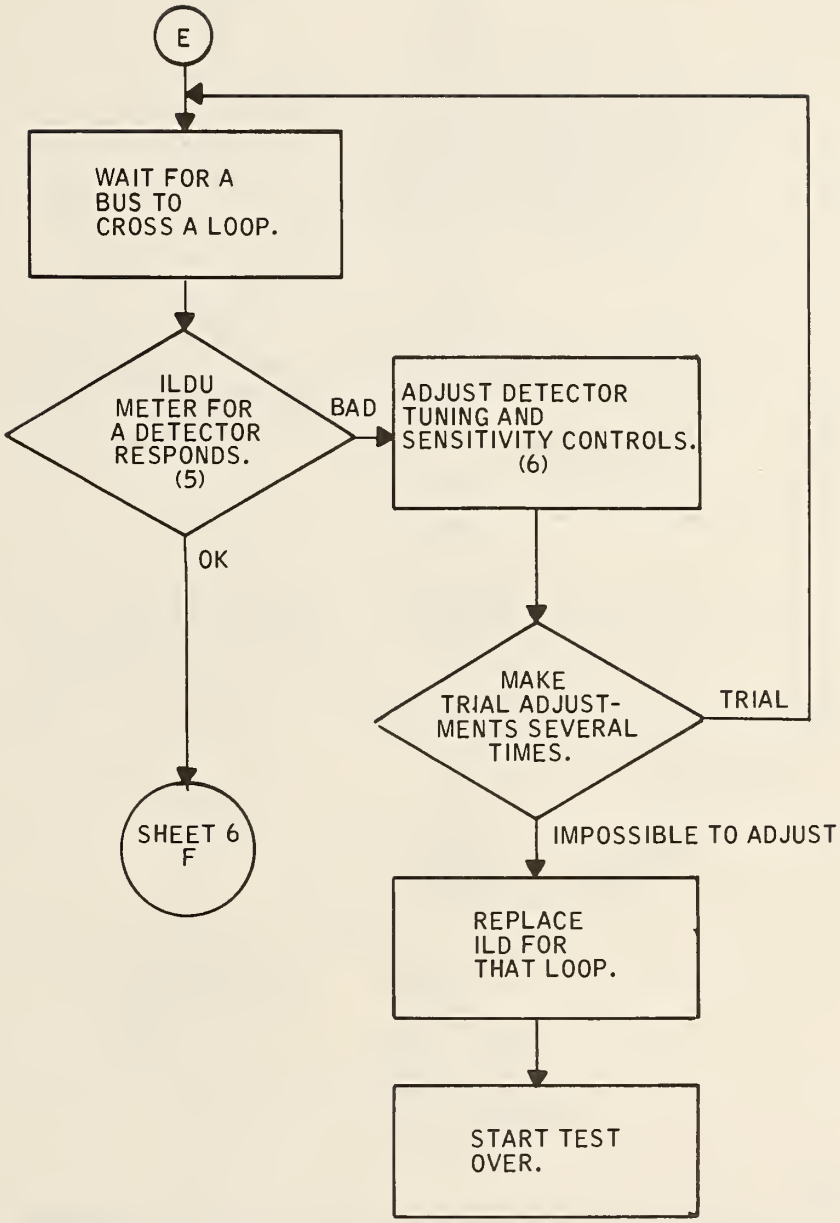


NOTES:

(3) SEE NOTES (1), (2) ON SHEET 2.

(4) IF REPLACING BCU DOES NOT RESOLVE PROBLEM, THEN DETECTORS 1-8, OR 9-16 CABLE MAY BE BAD.

Figure 26. Diagnostic Flow Chart (continued) (Sheet 4 of 11)

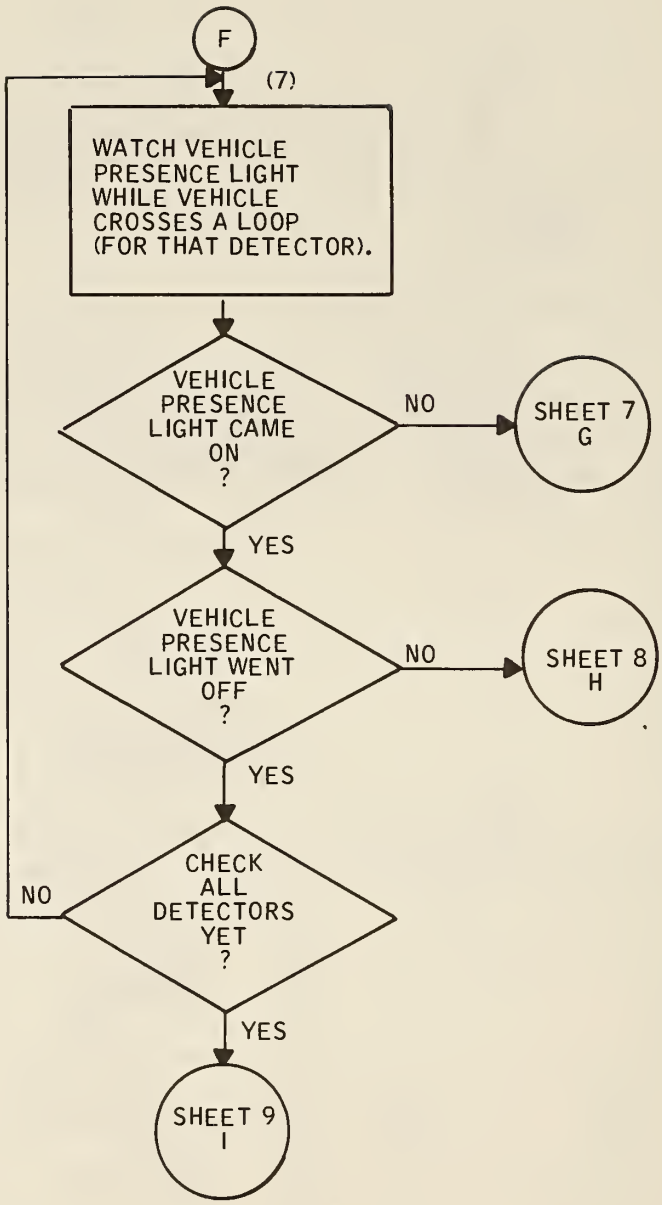


NOTES:

(5) METER RESPONSE SHALL BE PER PARAGRAPH 3.1.2.2.

(6) ADJUST PER PARAGRAPH 3.1.2.2.

Figure 26. Diagnostic Flow Chart (continued)
(Sheet 5 of 11)



NOTE:

(7) LENGTH OF VEHICLE PRESENCE LIGHT DURATION IS DEPENDENT ON VEHICLE PRESENCE SWITCH POSITION (FOR THAT DETECTOR). IF SWITCH IS IN "L" POSITION, THE LIGHT WILL BE ON FOR AS LONG AS A VEHICLE IS ON LOOP.

Figure 26. Diagnostic Flow Chart (continued)
(Sheet 6 of 11)

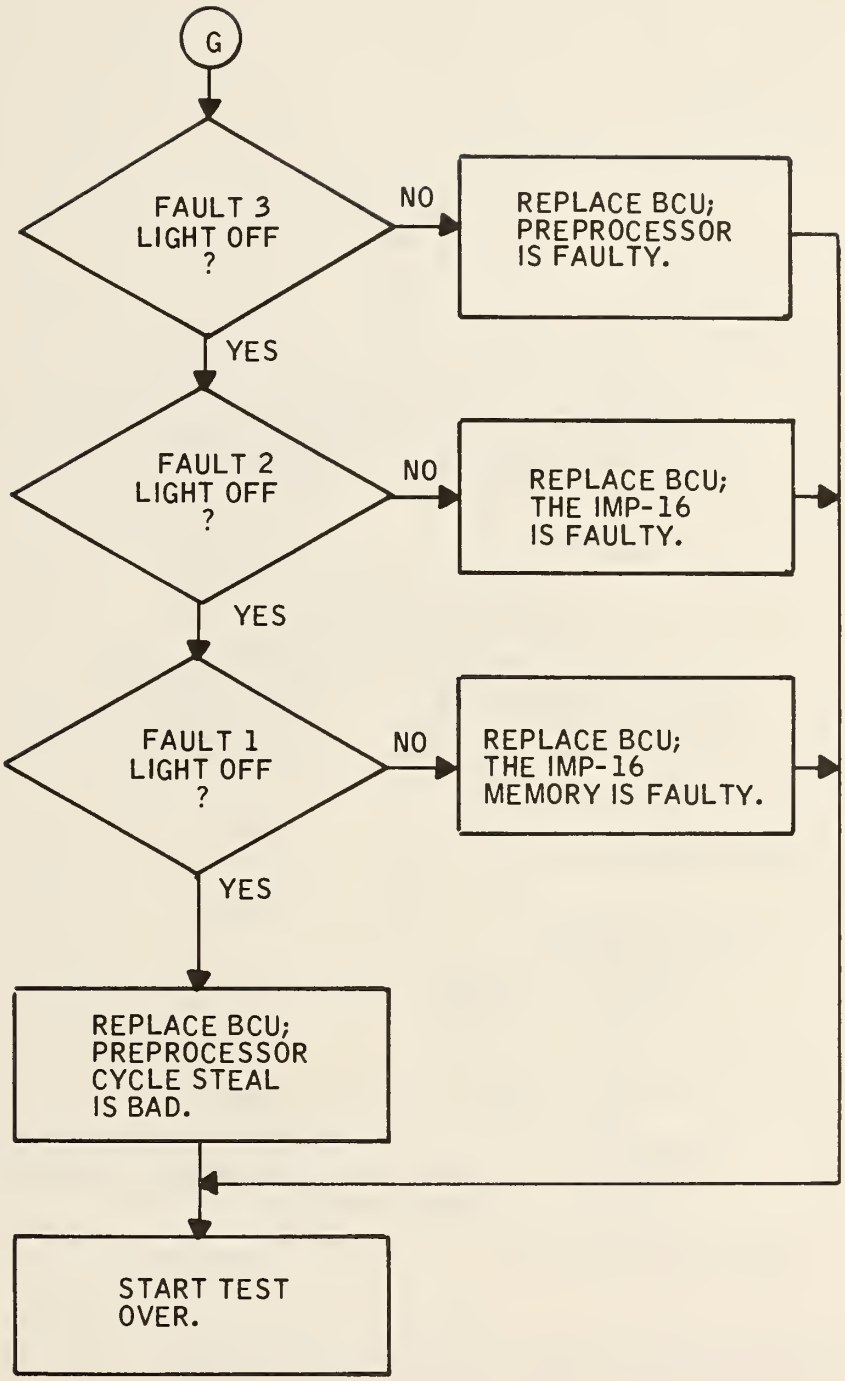


Figure 26. Diagnostic Flow Chart (continued)
(Sheet 7 of 11)

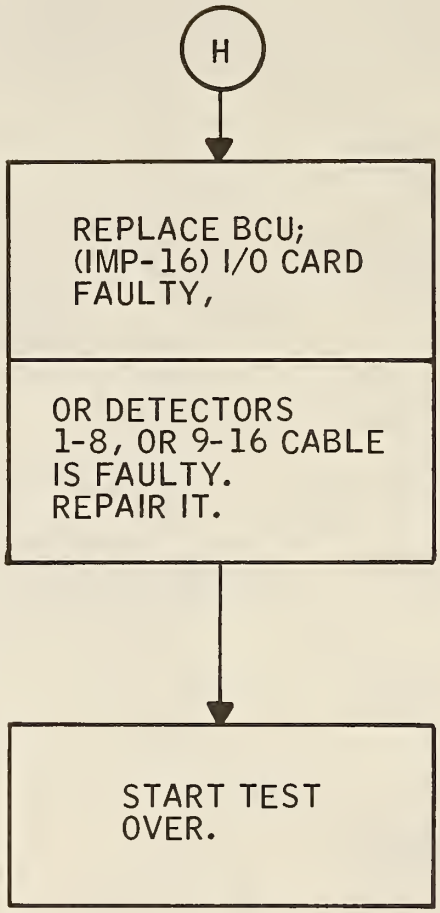


Figure 26. Diagnostic Flow Chart (continued)
(Sheet 8 of 11)

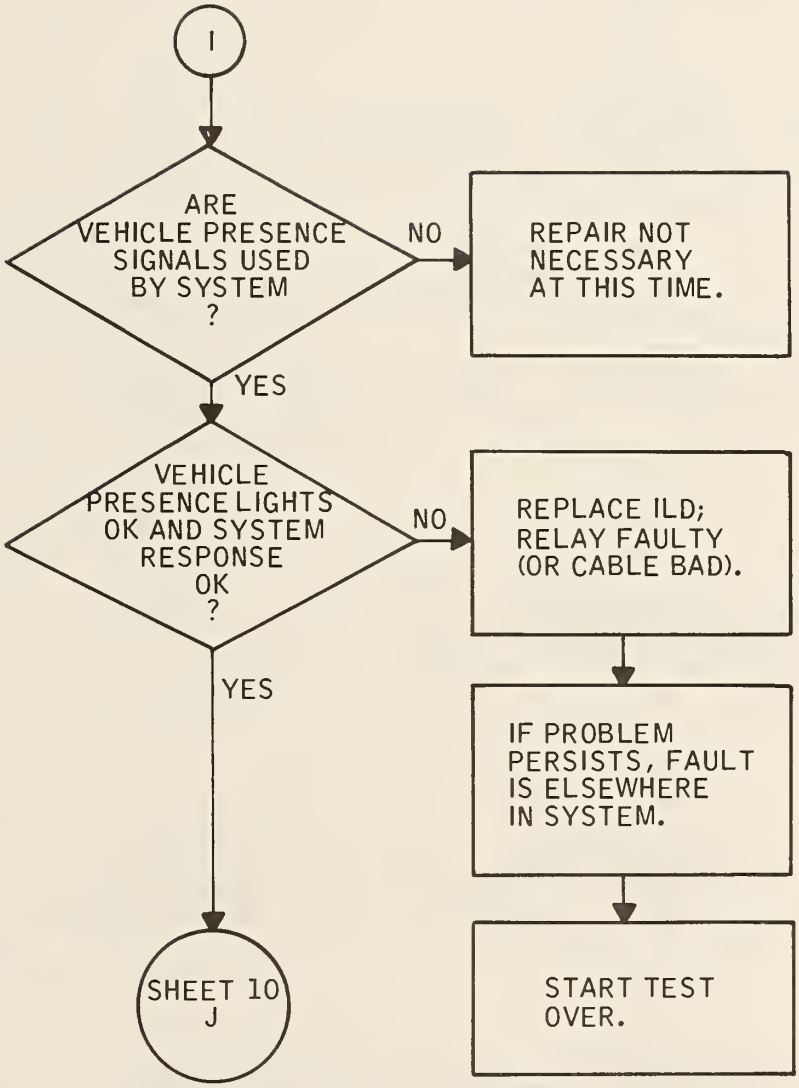


Figure 26. Diagnostic Flow Chart (continued)
(Sheet 9 of 11)

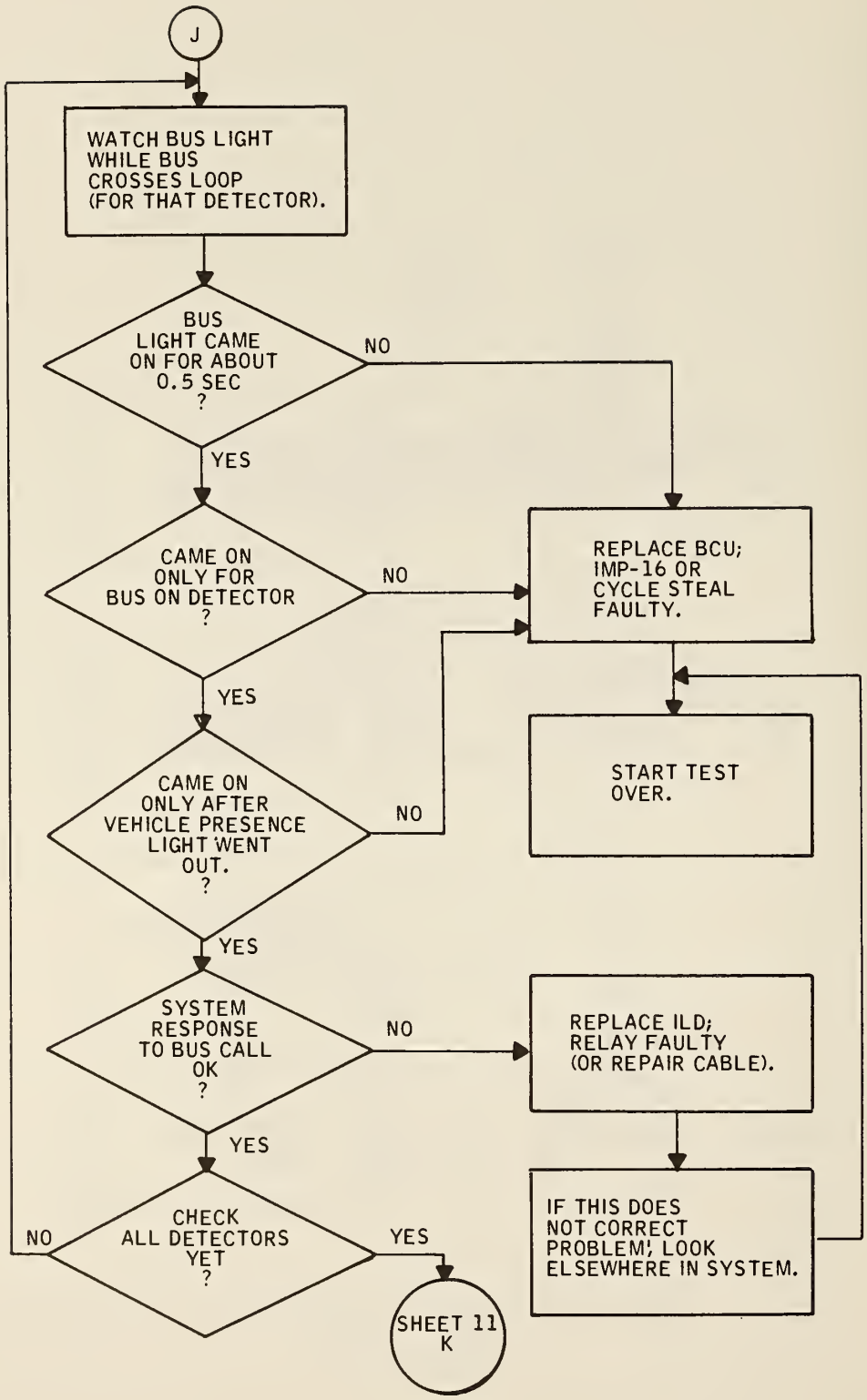


Figure 26. Diagnostic Flow Chart (continued)
(Sheet 10 of 11)

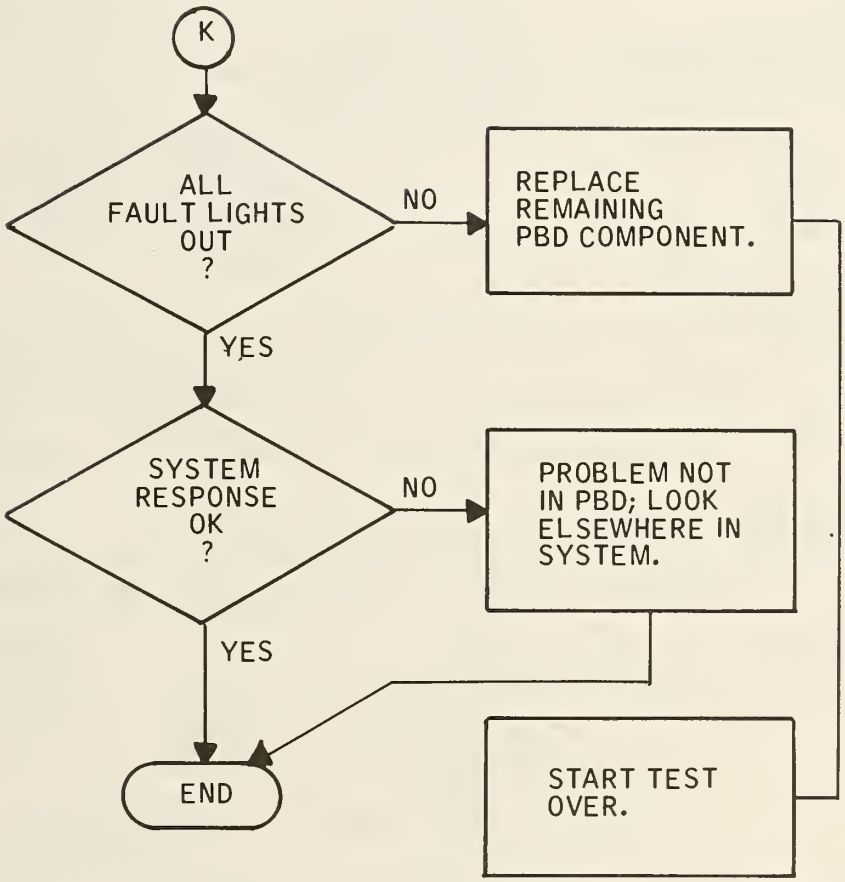


Figure 26. Diagnostic Flow Chart (continued)
(Sheet 11 of 11)

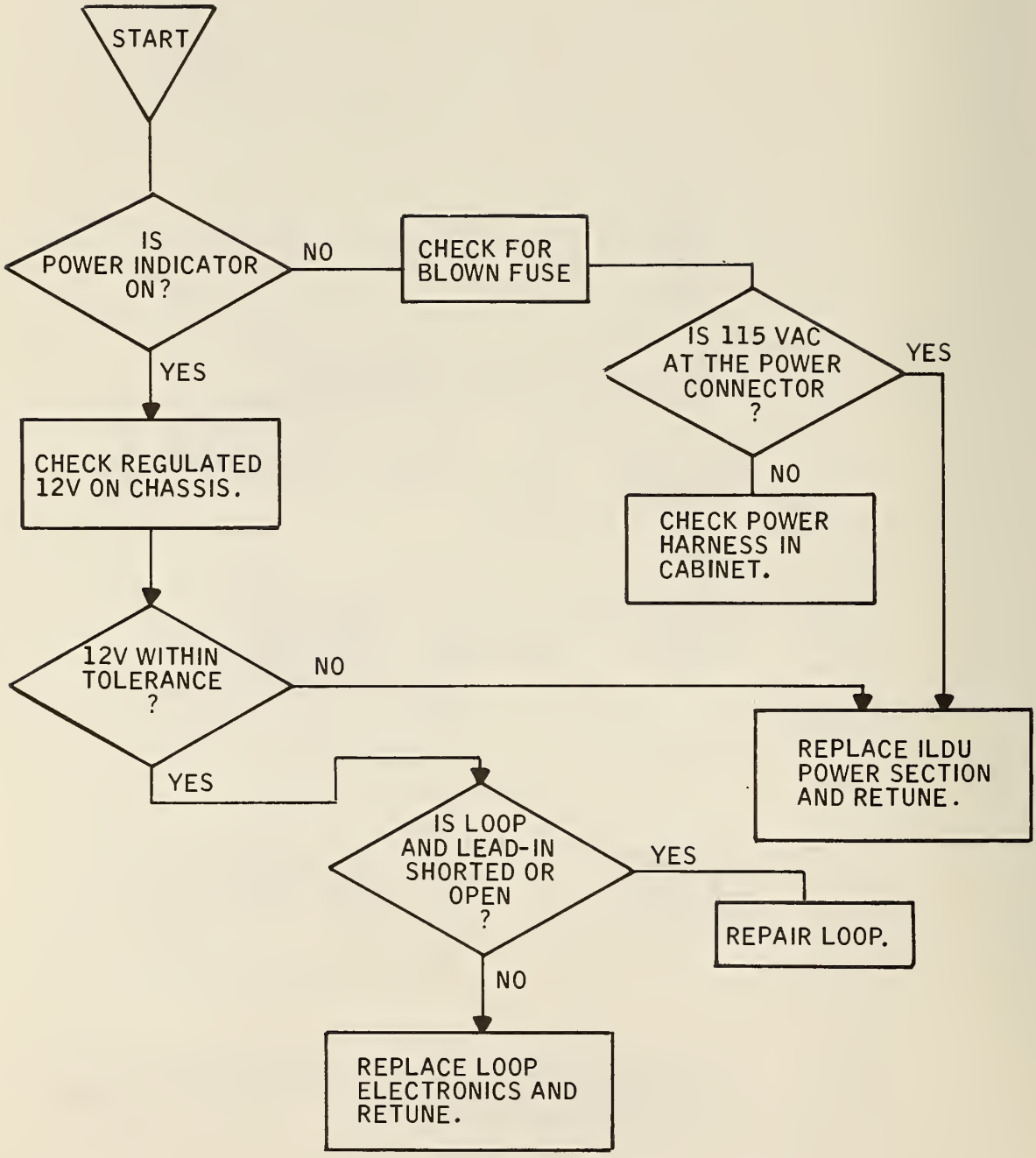


Figure 27. ILDU Tuning Flow Chart

SECTION 6
ASSEMBLY DRAWING AND PARTS LISTS

The following assembly drawings/parts are presented in this section:

Drwg. No.	Subject	Revision
YG1191A01	Detector, Bus	Original
28021592	Cable Assembly, Power - Loop Detector	A
28021595	Cable Assembly, BCU to Loop Detector	A
28021596	Cable, Loop Detector	A
28021597	Cable Assembly, Bus Classifier Unit	A
28021574	Bus Classifier Unit Assembly	A
28021579	Harness Assembly Power Supply	A
10063318	Printed-Circuit Assembly Motherboard, BCU	A
10063319 (Sheets 1, 2, 3)	Printed-Circuit Board Motherboard, BCU	Original
PL10059900	Bus Detector, PROM Memory	C
10059900	Printed-Circuit Assembly, PROM Memory, BCU	Original
10063320 (Sheets 1, 2, 3)	Printed-Circuit Board - PROM Memory, BCU	Original
PL10059899 (Sheet 1)	Bus Detector, I/O	A
PL10059899 (Sheet 2)	Bus Detector, I/O	D

Drwg. No.	Subject	Revision
10059899	Printed-Circuit Assembly I/O, BCU	Original
10063321 (Sheets 1, 2, 3)	Printed-Circuit Board - I/O	Original
PL10059904 (Sheet 1)	Preprocessor Control Decoding, Card 1	B
PL10059904 (Sheet 2)	Preprocessor Control Decoding, Card 1	D
10059904	Printed-Circuit Assembly, Preprocessor No. 1, BCU	Original
10063322 (Sheets 1, 2, 3)	Printed-Circuit Board, Preprocessor No. 1, BCU	Original
PL10059901	Cycle Steal Control/Address, Preprocessor Card No. 2	C
10059901	Printed-Circuit Assembly, Preprocessor No. 2, BCU	Original
10063323 (Sheets 1, 2, 3)	Printed-Circuit Board, Preprocessor No. 2	Original
28021581	Loop Detector Assembly	A
28021589	Cable Assembly, Power Supply	Original
28021590	Cable Assembly, Signal	A
PL10059903 (Sheet 1)	Loop Electronics	B
PL10059903 (Sheet 2)	Loop Electronics	A
PL10059903 (Sheet 3)	Loop Electronics	B

Drwg. No.	Subject	Revision
10059903	Printed-Circuit Assembly, Loop Electronics	Original
10063310 (Sheets 1, 2, 3)	Printed-Circuit Board - Loop Electronics	Original
10063324 (Sheets 1, 2)	Printed-Circuit Board - Thumbwheel	Original
PL10059902	Power Supply, Loop Electronics	D
10059902	Printed-Circuit Assembly - Relay and Power Supply, Loop Electronics	Original
10063315 (Sheets 1, 2, 3)	Printed-Circuit Board - Relay and Power Supply	Original
10063313	Printed-Circuit Assembly Mother-board, Loop Electronics	A
10063314 (Sheets 1, 2, 3)	Printed-Circuit Board - Loop Electronics Motherboard	Original
10063311	Printed-Circuit Assembly, Extender Loop Electronics	Original
10063312 (Sheets 1, 2, 3)	Printed-Circuit Board - Extender	Original

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM

HONEYWELL PART NO.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

THIS SYSTEM CONSISTS OF THE FOLLOWING:

BUS CLASSIFIER UNIT ASSY	28021574
LOOP DETECTOR ASSY	28021581
CABLE ASSY, POWER-LOOP DETECTOR	28021592
CABLE ASSY, BCU TO LOOP DETECTOR	28021595
CABLE, LOOP DETECTOR	28021596
CABLE ASSY, BUS CLASSIFIER UNIT	28021597

NEXT ASSY	USED ON
APPLICATION	

TOLERANCES UNLESS NOTED OTHERWISE: .X ±, .XX ±, .XXX ±; 90° FORMED ANGLES +2° −1°

FINISH—NOTE

MATL

DRAFTSMAN	[illegible]	10-17-77
CHECK		
DEV ENGR		
PROJ ENGR		
RELIABILITY		

CONTRACT NO.

HONEYWELL INC. AEROSPACE AND DEFENSE GROUP

☐ AERO MPLS ☐ AERO ST PETERSBURG ☐ ORO SEATTLE ☐ ORO HOPKINS ☐ ORO MONTGOMERYVILLE ■ S&R CTR MPLS ☐ RADIATION CTR BOSTON

DETECTOR, BUS

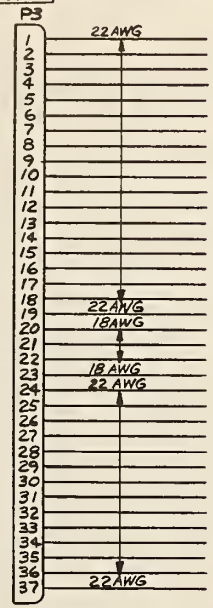
SIZE	CODE IDENT NO.	DRAWING NO.
B	27327	YG1191A01

SCALE | WT | SHEET

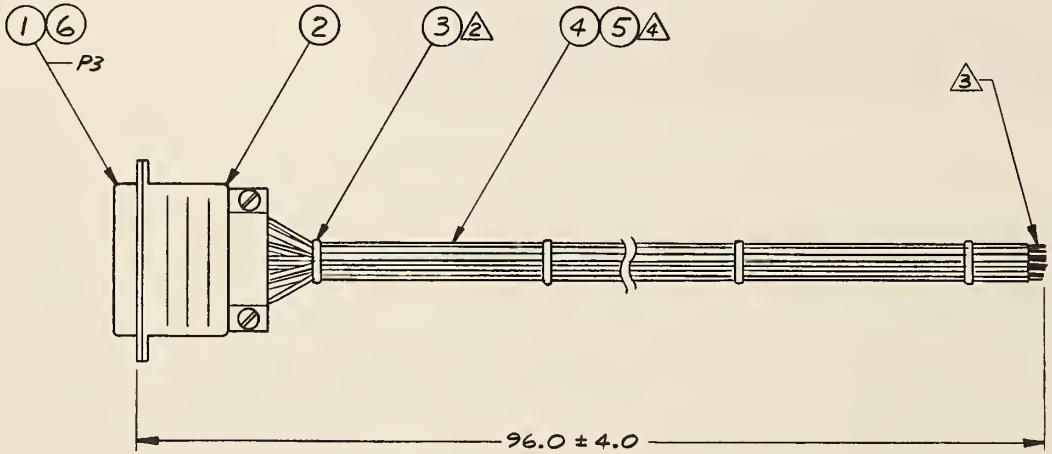
DF-4 7-71 V400

DASH NO.
-001

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	REV	8-5-77	



SCHEMATIC DIAGRAM



QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION		REMARKS	ITEM NO
37	66504-9	CONTACT, SOCKET		AMP	6
AR	1	LEADWIRE 22 AWG			5
AR	1	LEADWIRE 18 AWG			4
AR	TY-23M	CABLE TIE		T&B	3
1	DD-24661	JUNCTION SHELL		CINCH	2
1	205209-1	CONNECTOR, RECEPTACLE	P3	AMP	1

4 HEAT STAMP CONNECTOR REF DES AND PIN NO. EVERY 3.0±0.5

3 - STRIP INSULATION 3/8 INCH AND TIN

2 - CABLE TIE EVERY 3 INCHES MAX

1 - ALL LEADWIRE MIN 19 STRANDS PER MIL-W-16878D, TYPE B OR D, 600V, 105°C, VINYL-NYLON JACKET OR IRRADIATED CROSS LINKED POLYVINYL CHLORIDE. SEE SCHEMATIC DIAGRAM.

REFERENCE	NEXT ASSY	USED ON
( )		
( )		
( )		
( )		
( )	28021581	LOOP DET

-001 THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE: X ±, .XX ±, .XXX ±; 90° FORMED ANGLES -1° +2°

MATERIAL

FINISH—SEE NOTE

DRAWN BY D.R. Rosen 6-3-77; CHECKER; DEV ENGR; ENGRG MGT; CONTRACT NO; AGENCY APPROVAL

HONEYWELL INC — TRAFFIC MANAGEMENT CENTER

CABLE ASSY, POWER - LOOP DETECTOR

SIZE C | FSCM NO | DWG NO 28021592

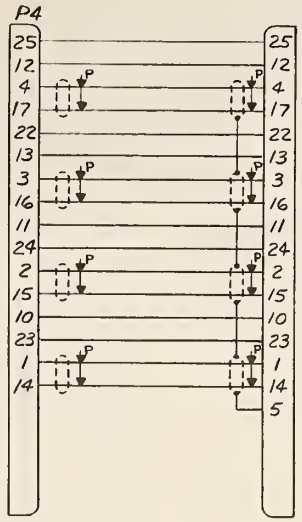
SCALE 1/1 | SHEET 1 OF

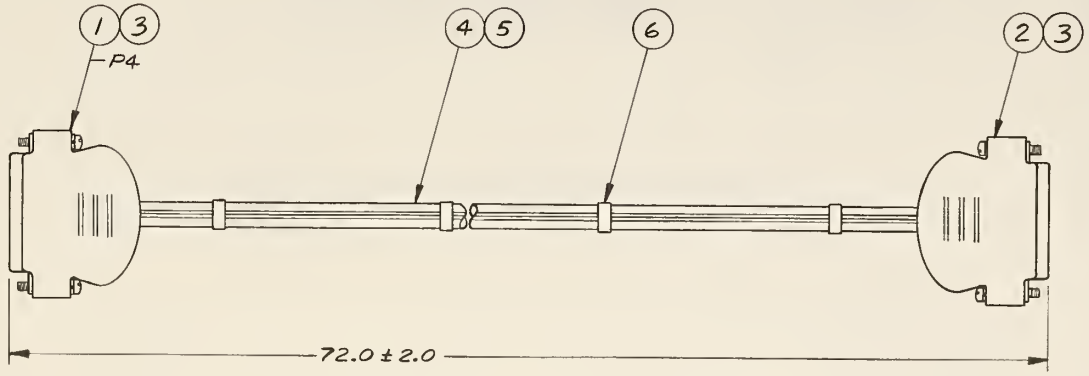
CONTROL

TMC-C 1/77

DASH NO. -001

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	REVISE	10-14-77	[illegible]





QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	REMARKS	ITEM NO
AR	TY-23M	CABLE TIE	T & B	6
AR	/1\	LEADWIRE 22 AWG		5
AR	3221	LEADWIRE 22 AWG TW SHLD PR	OR EQUIV ALPHA	4
2	DB-51226-1	HOOD, CONNECTOR	CINCH	3
1	DB-25P	CONNECTOR, MALE	CINCH	2
1	DB-25S	CONNECTOR, FEMALE	P4 CINCH	1

/1\ - ALL LEADWIRE MIN 19 STRANDS PER MIL-W-16878D, TYPE B OR D, 600V, 105°C, VINYL-NYLON JACKET OR IRRADIATED CROSS LINKED PVC

REFERENCE	NEXT ASSY	USED ON
( )		
( )		
( )		
( )		
( )		BCU

-001 THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE: X ±, XX ±, XXX ±; 90° FORMED ANGLES ±1° ±2°

MATERIAL

FINISH – SEE NOTE

DRAWN BY [illegible] 42972; CHECKER; DES ENGR; ENGRG MGT

CONTRACT NO

AGENCY APPROVAL

HONEYWELL INC — TRAFFIC MANAGEMENT CENTER

CABLE ASSY, BCU TO LOOP DET

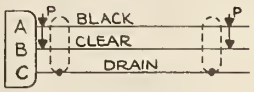
SIZE C; FSCM NO; DWG NO 28021595; SCALE 1/1; SHEET 1 OF

CONTROL

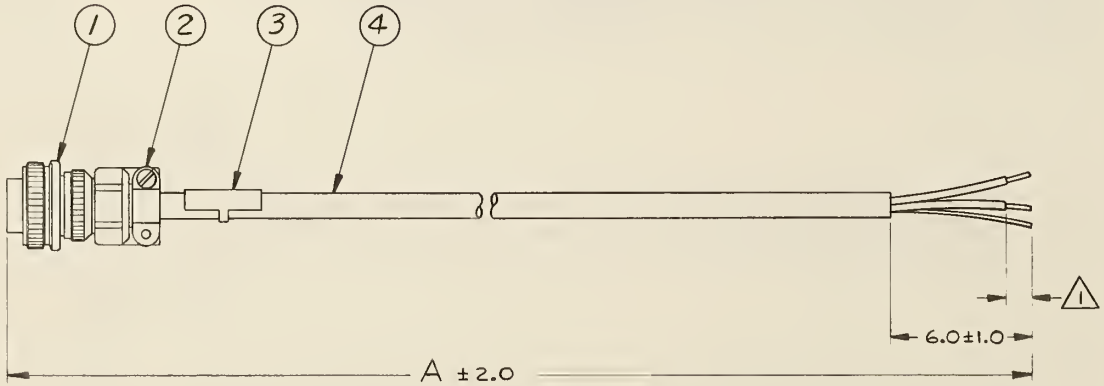
TMC C 1/77

DASH NO.	A
-001	96.0
-002	120.0
-003	60.0

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	REV	8-5-77	



SCHEMATIC DIAGRAM



QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION		REMARKS	ITEM NO.
AR	8720	CABLE, 2 COND, SHLD-14 AWG	BELDEN		4
1	TY-51M	IDENT MARKER	T&B		3
1	MS3057-6A	CABLE CLAMP			2
1	MS3106A-14S-7S	CONNECTOR			1

2 - BAG AS ASSY AND MARK WITH PART NO.

1 - STRIP INSULATION 3/8 INCH AND TIN

REFERENCE	NEXT ASSY	USED ON
( )		
( )		
( )		
( )		
( )		LOOP DET

THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE: .X ± .XX ± .XXX ± 90° FORMED ANGLES -1° +2°

MATERIAL

FINISH—SEE NOTE

DRAWN BY W.E. Carson 8-2-77

CHECKER

DEV ENGR

ENGRG MGT

CONTRACT NO.

AGENCY APPROVAL

HONEYWELL INC — TRAFFIC MANAGEMENT CENTER

CABLE, LOOP DETECTOR

SIZE C | FSCM NO | DWG NO. 28021596

SCALE 1/1 | SHEET 1 OF

CONTROL

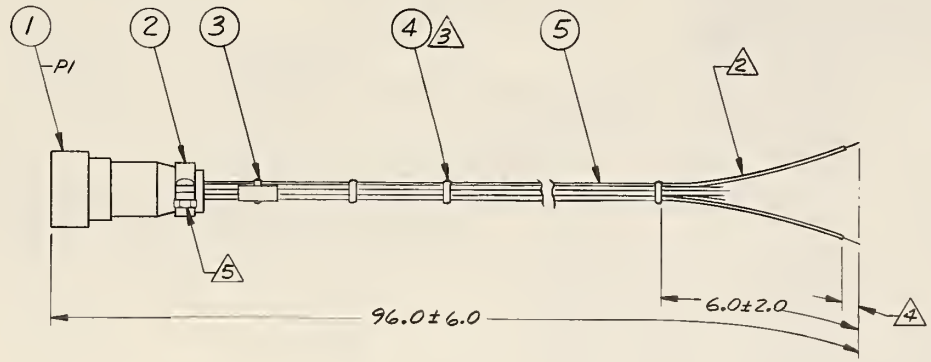
TMC-C 1/77

DASH NO. -001

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	REV	8-5-77	

P1		
A	115V HI	16 AWG
B	115V LO	16 AWG
C	GND	16 AWG
D	FAULT 1	22 AWG
E	FAULT 2	22 AWG
F	FAULT 3	22 AWG
G	E/T RESET	22 AWG

SCHEMATIC DIAGRAM



5. CLIP SCREW FLUSH WITH NUT AFTER ASSEMBLY
4. STRIP INSULATION 3/8 INCH AND TIN
3. CABLE TIE EVERY 3.0 MIN INCHES
2. HEAT STAMP CONNECTOR PIN LETTER EVERY 3.0 ± .5 INCHES
1. ALL LEADWIRE MIN 19 STRANDS PER MIL-W-16878D, TYPE B OR D, 600V, 105°C, VINYL-NYLON JACKET OR IRRADIATED CROSS LINKED POLYVINYL CHLORIDE. SEE SCHEMATIC DIAGRAM FOR WIRE SIZE

QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	REMARKS	ITEM NO
AR	1	LEADWIRE		5
AR	TY-524M	CABLE TIE	T & B	4
1	TY-551M	IDENT MARKER	T & B	3
1	MS3057-16A	CABLE CLAMP		2
1	MS3106A-24-27S	CONNECTOR, PLUG	P1	1

-001 THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE: .X ± .XX ± .XXX ± 90° FORMED ANGLES -1° +2°

MATERIAL

FINISH—SEE NOTE

DRAWN BY R. Hanson 4-26-77
CHECKER
DEV ENGR
ENGRG MGT
CONTRACT NO
AGENCY APPROVAL

HONEYWELL INC — TRAFFIC MANAGEMENT CENTER

CABLE ASSEMBLY, BUS CLASSIFIER UNIT

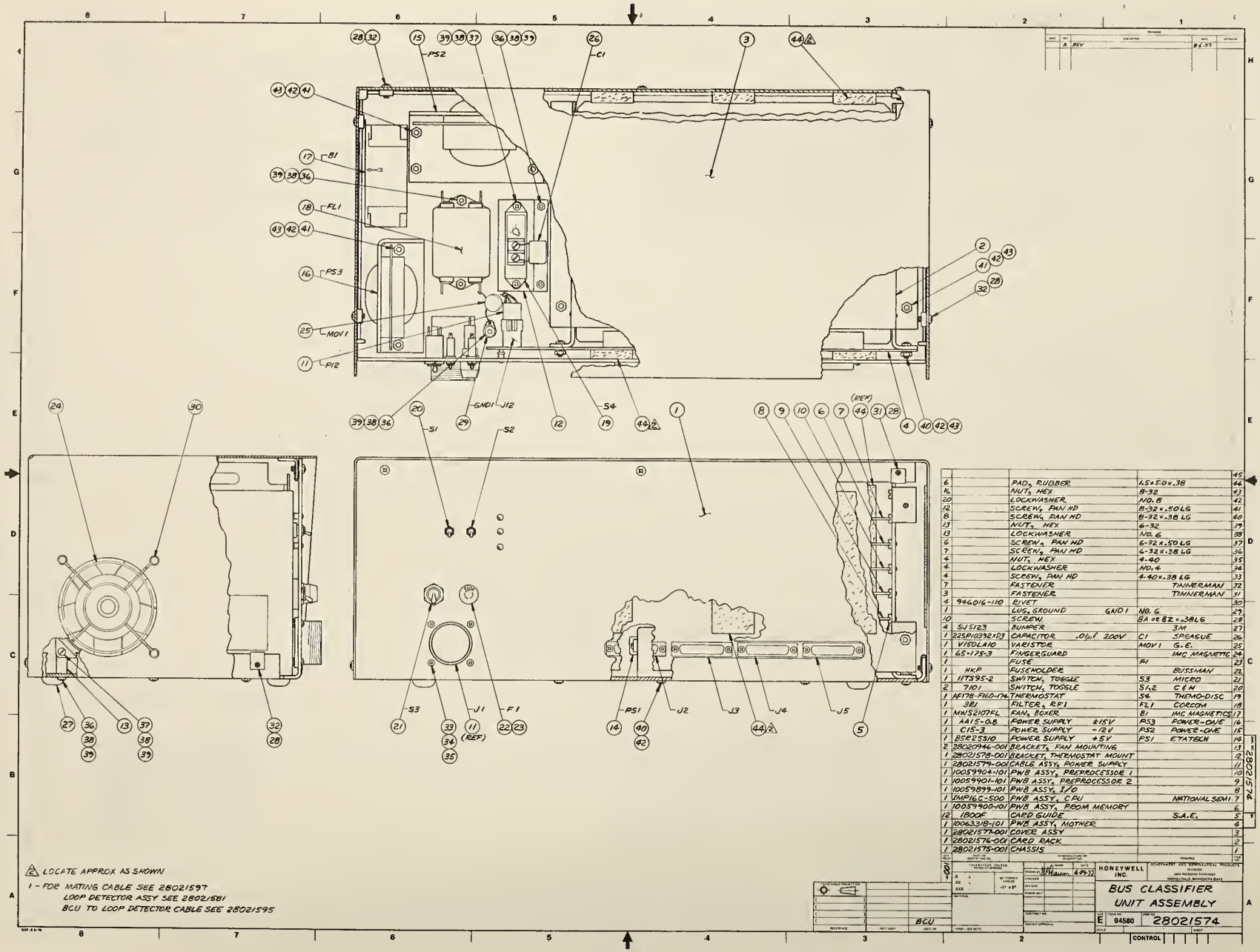
SIZE C | FSCM NO | DWG NO 28021597

SCALE NONE | SHEET 1 OF

CONTROL

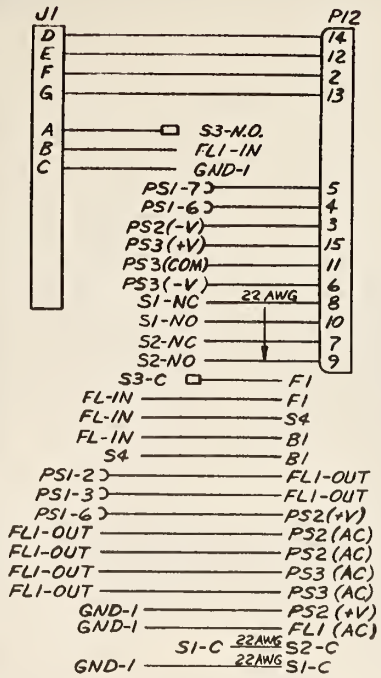
REFERENCE	NEXT ASSY	USED ON
( )		
( )		
( )		
( )		
( )		BCU

TMC C 1/77

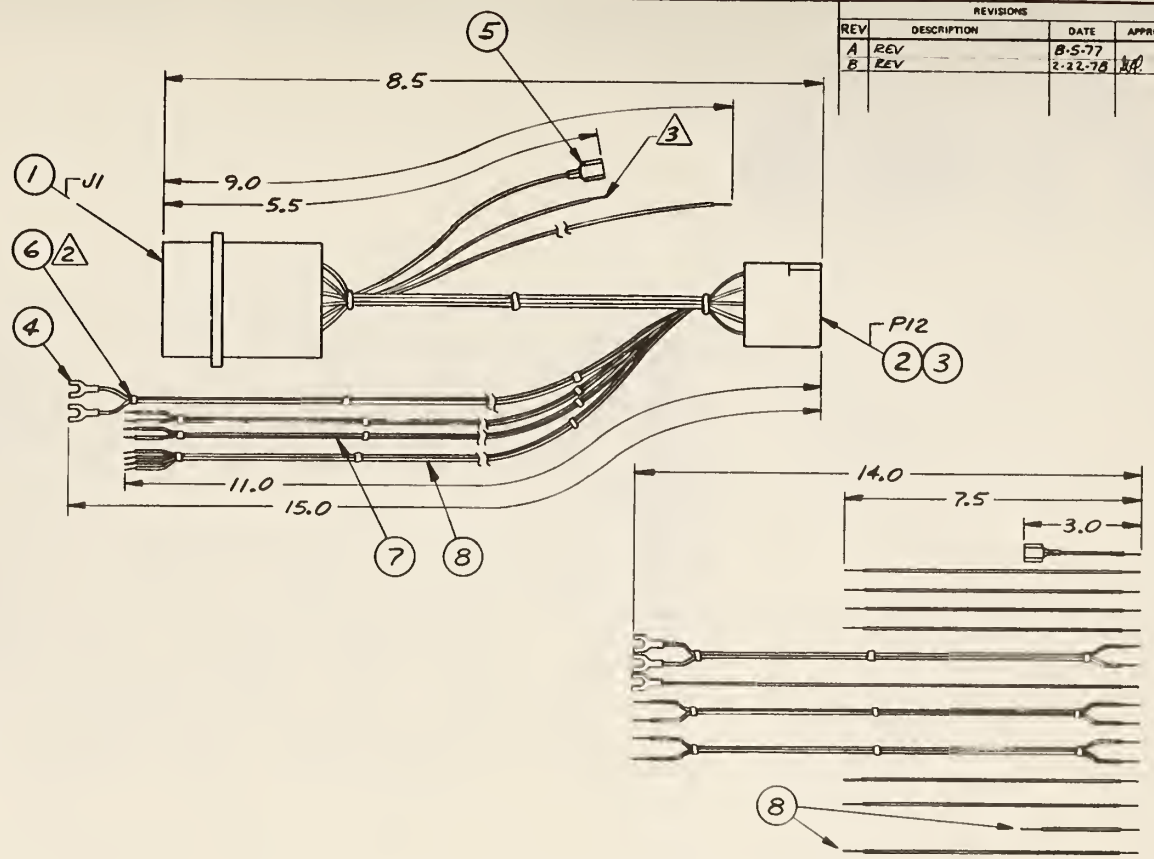


6		PAD, RUBBER	1.5×5.0×.38		45
16		NUT, HEX	8-32		43
20		LOCKWASHER	NO. 8		42
12		SCREW, PAN HD	8-32×.50 LG		41
8		SCREW, PAN HD	8-32×.38 LG		40
13		NUT, HEX	6-32		39
13		LOCKWASHER	NO. 6		38
6		SCREW, PAN HD	6-32×.50 LG		37
7		SCREW, PAN HD	6-32×.38 LG		36
4		NUT, HEX	4-40		35
4		LOCKWASHER	NO. 4		34
4		SCREW, PAN HD	4-40×.38 LG		33
7		FASTENER		TINNERMAN	32
3		FASTENER		TINNERMAN	31
4	984016-110	RIVET			30
1		LUG, GROUND GND1	NO. 6		29
10		SCREW	8A 32 8Z×.38LG		28
4	SJ5123	BUMPER	3M		27
1	225P10392X03	CAPACITOR .01μf 200V	C1	SPRAGUE	26
1	V150LA10	VARISTOR	MOV1	G.E.	25
1	65-175-3	FINGERGUARD		IMC MAGNETIC	24
1		FUSE	F1		23
1	HKP	FUSEHOLDER		BUSSMAN	22
1	11TS95-2	SWITCH, TOGGLE	S3	MICRO	21
2	7101	SWITCH, TOGGLE	S1,2	C&N	20
1	AE178-F160-174	THERMOSTAT	S4	THERMO-DISC	19
1	3EI	FILTER, RFI	FL1	COEGON	18
1	MK32107FL	FAN, ROKER	B1	IMC MAGNETICS	17
1	AA15-0.8	POWER SUPPLY ±15V	PS3	POWER-ONE	16
1	C15-3	POWER SUPPLY -12V	PS2	POWER-ONE	15
1	BSR25S10	POWER SUPPLY +5V	PS1	ETATSCH	14
2	28020946-001	BRACKET, FAN MOUNTING			13
1	28021578-001	BRACKET, THERMOSTAT MOUNT			12
1	28021579-001	CABLE ASSY, POWER SUPPLY			11
1	100599904-101	PWB ASSY, PREPROCESSOR 1			10
1	100599901-101	PWB ASSY, PREPROCESSOR 2			9
1	100599899-101	PWB ASSY, I/O			8
1	UMP16C-500	PWB ASSY, CPU		NATIONAL SEMI	7
1	100599900-101	PWB ASSY, PROM MEMORY			6
12	1B00F	CARD GUIDE		S.A.E.	5
1	1006331B-101	PWB ASSY, MOTHER			4
1	28021577-001	COVER ASSY			3
1	28021576-001	CARD RACK			2
1	28021575-001	CHASSIS			1

DASH NO. -001



SCHEMATIC DIAGRAM



REV	DESCRIPTION	DATE	APPROVED
A	REV	8-5-77	
B	REV	2-22-78	

4 - SCHEMATIC DIAGRAM SYMBOLS:

- QUICK DISCONNECT LUG (ITEM 5)
- OPEN SPADE LUG (ITEM 4)

4 - BAG AS ASSEMBLY AND MARK WITH PART NO.

3 - STRIP INSULATION 3/8 INCH AND TIN

2 - CABLE TIE EVERY 3 INCHES

1 - ALL LEADWIRE MIN 19 STRANDS PER MIL-W-16878 D, TYPE B OR D, 600V, 105°C, VINYL-NYLON JACKET OR IRRADIATED CROSS LINKED POLYVINYL CHLORIDE

QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	REMARKS	ITEM NO
AR		LEADWIRE 22 AWG		8
AR	1	LEADWIRE 16 AWG		7
AR	TY-23M	CABLE TIE	T&B	6
2		LUG, QUICK DISCONNECT		5
5		LUG, SPADE - OPEN	NO.8	4
10	02-09-1134	CONTACT, FEMALE	MOLEX	3
1	03-09-1152	RECEPTACLE	P12 MOLEX	2
1	MS3102A-24-27P	CONNECTOR	J1	1

-001

THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE: X = .3, XX =, XXX =, BOTFORMED ANGLES ±1° ±2°

MATERIAL

FINISH - SEE NOTE

DRAWN BY [illegible] 4-25-77

CHECKER

DEV ENGR

ENGRG MGT

CONTRACT NO

AGENCY APPROVAL

HONEYWELL INC — TRAFFIC MANAGEMENT CENTER

HARNESS ASSEMBLY, POWER SUPPLY

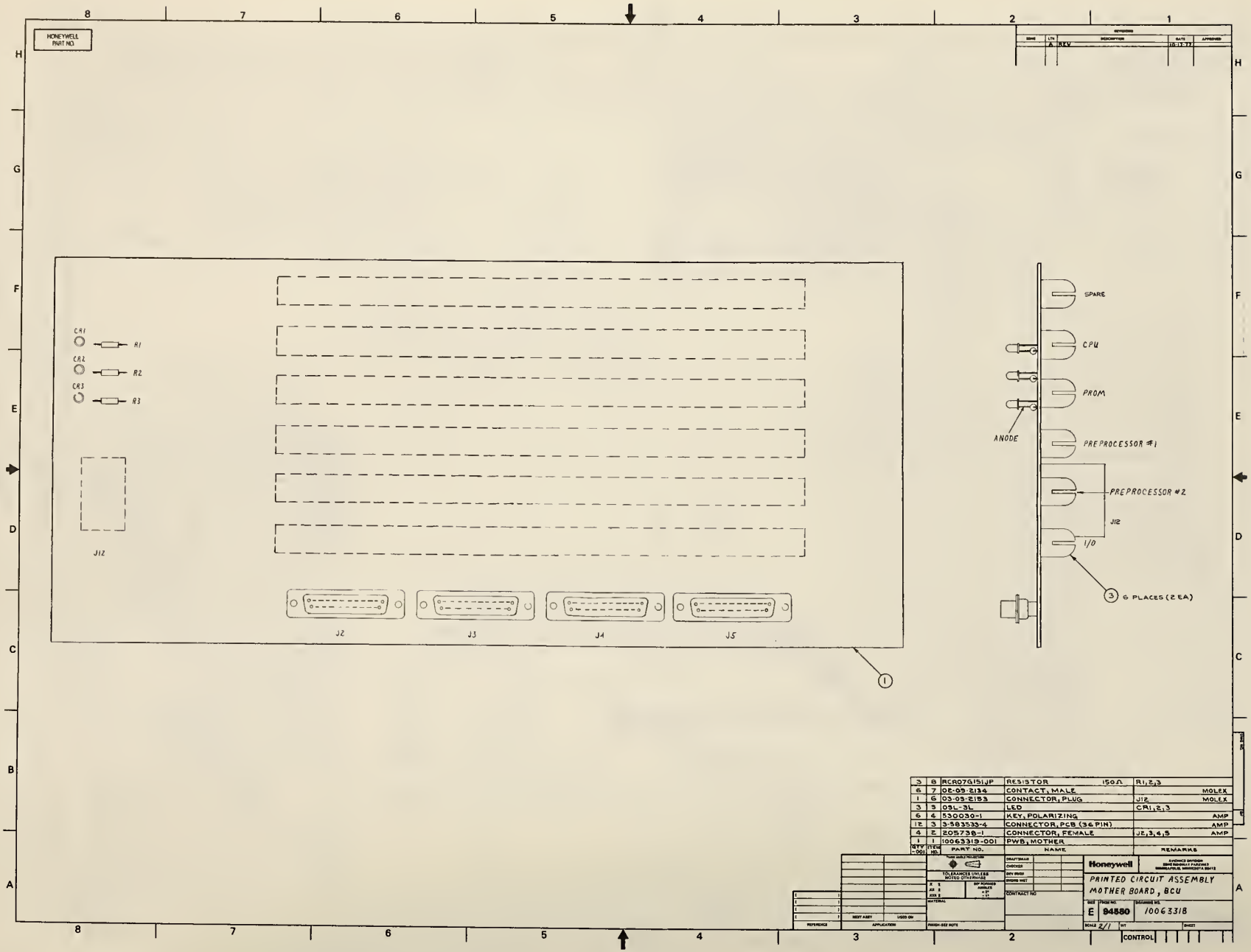
SIZE C — FSCM NO — DWG NO 28021579

SCALE 1/1 — SHEET 1 OF

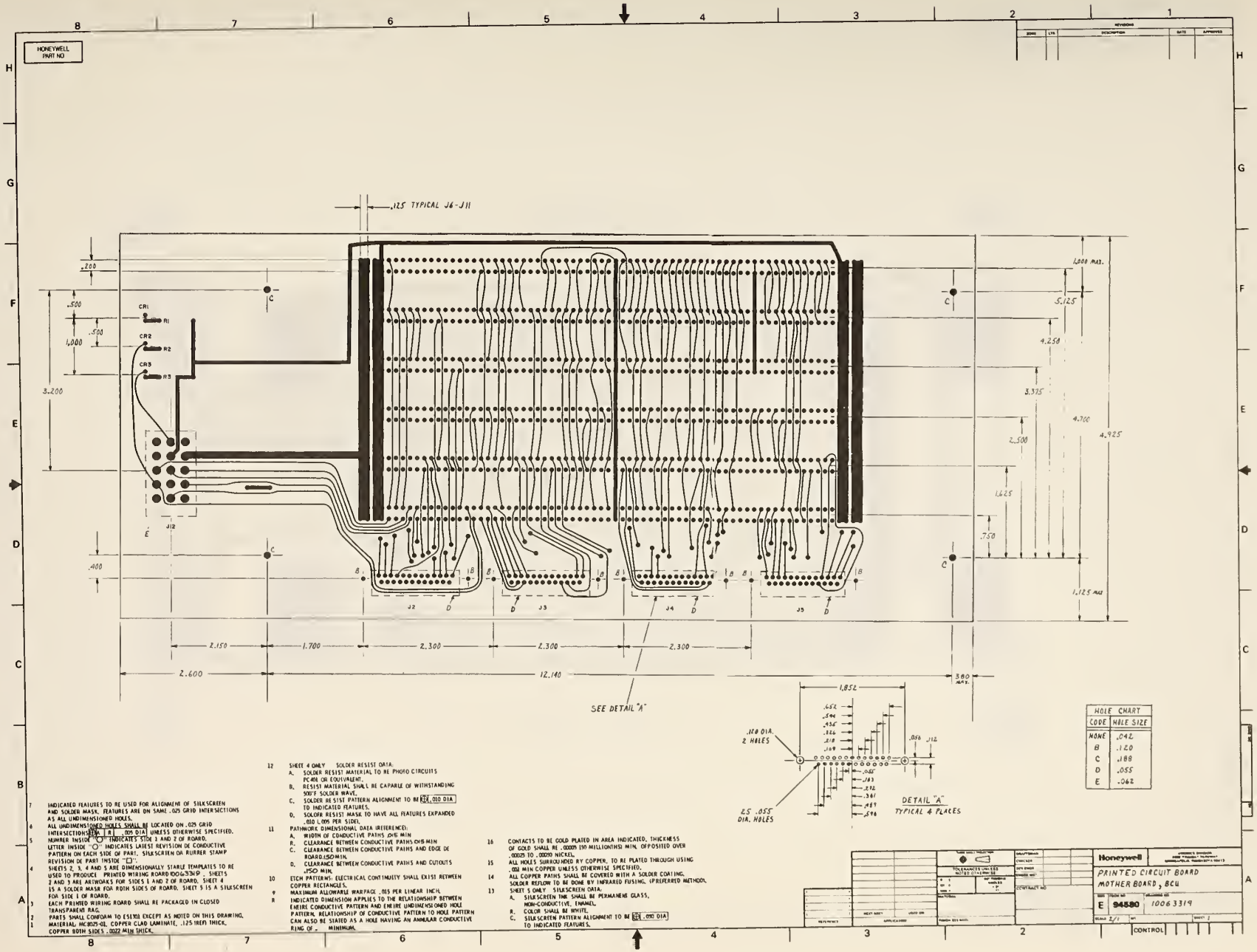
REFERENCE	NEXT ASSY	USED ON
	28021574	BCU

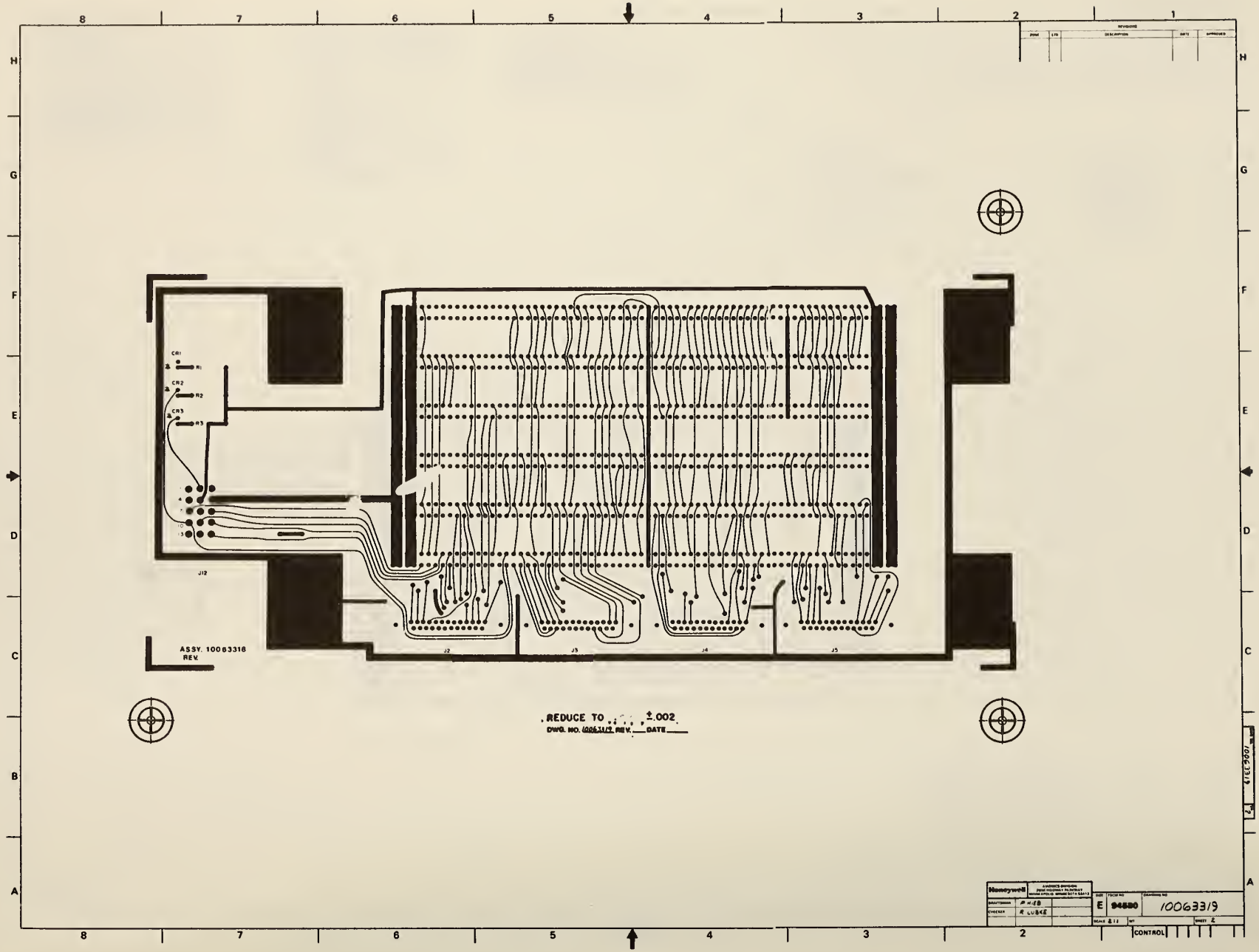
CONTROL A 309B

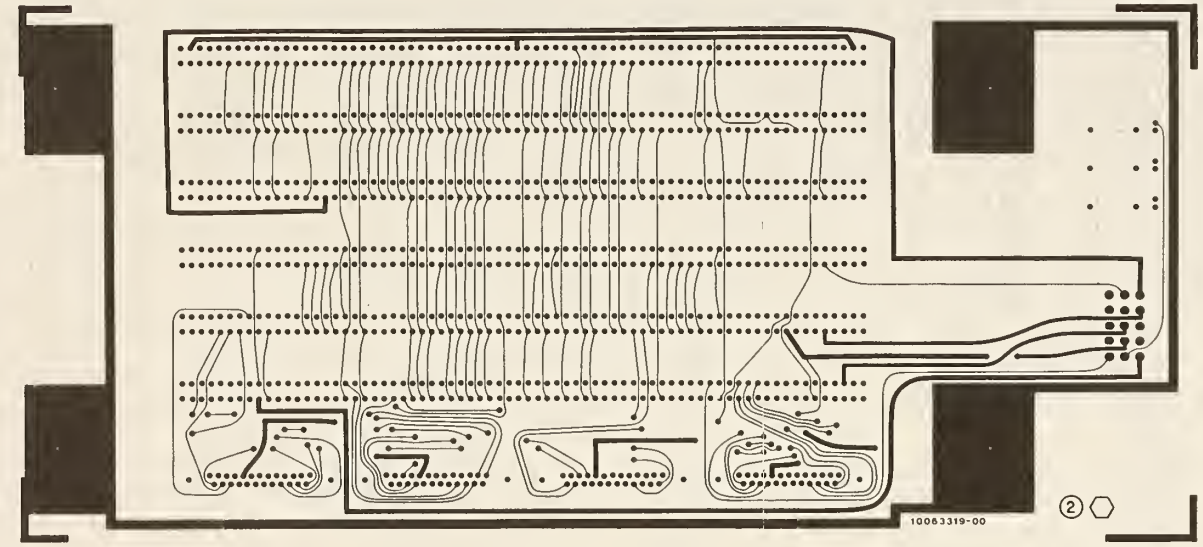
TMC-C 1/77



QTY -001	ITEM NO.	PART NO.	NAME	REMARKS
3	8	RCR07G151JP	RESISTOR 150Ω	R1,2,3
6	7	02-09-2134	CONTACT, MALE	MOLEX
1	6	03-09-2153	CONNECTOR, PLUG	J12, MOLEX
3	3	05L-3L	LED	CR1,2,3
6	4	530030-1	KEY, POLARIZING	AMP
12	3	3-583533-4	CONNECTOR, PCB (36 PIN)	AMP
4	2	205738-1	CONNECTOR, FEMALE	J2,3,4,5 AMP
1	1	10063319-001	PWB, MOTHER	


HONEYWELL PART NO
REVISIONS
.125 TYPICAL J6-J11
CR1
R1
CR2
R2
CR3
R3
J12
J2
J3
J4
J5
SEE DETAIL "A"
2.150
1.700
2.300
2.300
2.300
2.600
12.140
3.200
1.000 MAX.
5.125
4.250
3.375
2.500
1.625
.750
4.700
4.925
1.125 MAX
.560 MAX.
1.852
.120 DIA. 2 HOLES
.125 .055 DIA. HOLES
DETAIL "A" TYPICAL 4 PLACES
HOLE CHART
CODE HOLE SIZE
NONE .042
B .120
C .188
D .055
E .062
7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.
6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS ±.005 .005 DIA UNLESS OTHERWISE SPECIFIED.
5 NUMBER INSIDE "O" INDICATES SIDE 1 AND 2 OF BOARD. LETTER INSIDE "O" INDICATES LATEST REVISION DE CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION DE PART INSIDE "□".
4 SHEETS 2, 3, 4 AND 5 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCE PRINTED WIRING BOARD 10063319 . SHEETS 2 AND 3 ARE ARTWORKS FOR SIDES 1 AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE 1 OF BOARD.
3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.
2 PARTS SHALL CONFORM TO ES1031 EXCEPT AS NOTED ON THIS DRAWING.
1 MATERIAL MC8025-01, COPPER CLAD LAMINATE, .125 REF) THICK. COPPER BOTH SIDES .0027 MIN THICK.
12 SHEET 4 ONLY SOLDER RESIST DATA.
A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC401 OR EQUIVALENT.
B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
C. SOLDER RESIST PATTERN ALIGNMENT TO BE ±.010 DIA TO INDICATED FEATURES.
D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 L.005 PER SIDE.
11 PATHWORK DIMENSIONAL DATA (REFERENCE):
A. WIDTH OF CONDUCTIVE PATHS .015 MIN
B. CLEARANCE BETWEEN CONDUCTIVE PATHS .015 MIN
C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE DE BOARD .150 MIN.
D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS .150 MIN.
10 ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.
9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.
8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENEIRE CONDUCTIVE PATTERN AND ENEIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF . MINIMUM.
16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00005 (50 MILLIONTHS) MIN. OPPOSITED OVER .00025 TO .00050 NICKEL.
15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.
14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).
13 SHEET 5 ONLY SILKSCREEN DATA.
A. SILKSCREEN INK SHALL BE PERMANENE GLASS, NON-CONDUCTIVE, ENAMEL.
B. COLOR SHALL BE WHITE.
C. SILKSCREEN PATTERN ALIGNMENT TO BE ±.010 DIA TO INDICATED FEATURES.
Honeywell
PRINTED CIRCUIT BOARD
MOTHER BOARD, BCU
E 94580 10063319
CONTROL


CR1
R1
CR2
R2
CR3
R3
J12
J2
J3
J4
J5
ASSY. 10063318
REV.
REDUCE TO ±.002
DWG. NO. 10063319 REV. DATE
Honeywell
DRAFTSMAN
CHECKER
R. LUBKE
E
94580
10063319
SCALE 8:1
SHEET 2
CONTROL



REDUCE TO ±.002

DWG NO 10063319 REV ___ DATE ___

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

Honeywell

DRAFTSMAN P. NEB

CHECKER R. LUBKE

E 94580 10063319

SCALE 2:1 SHEET 3

CONTROL

Honeywell

PRINTED IN U. S. A.

SUPERSEDES
SUPERSEDED BY

ENGINEERING PARTS LIST

REV.	DATE	E.O.	REV.	DATE	E.O.
A	6-9-77				
B	10-6-77				
C	10-10-77				

BUS DETECTOR, PROM. MEM

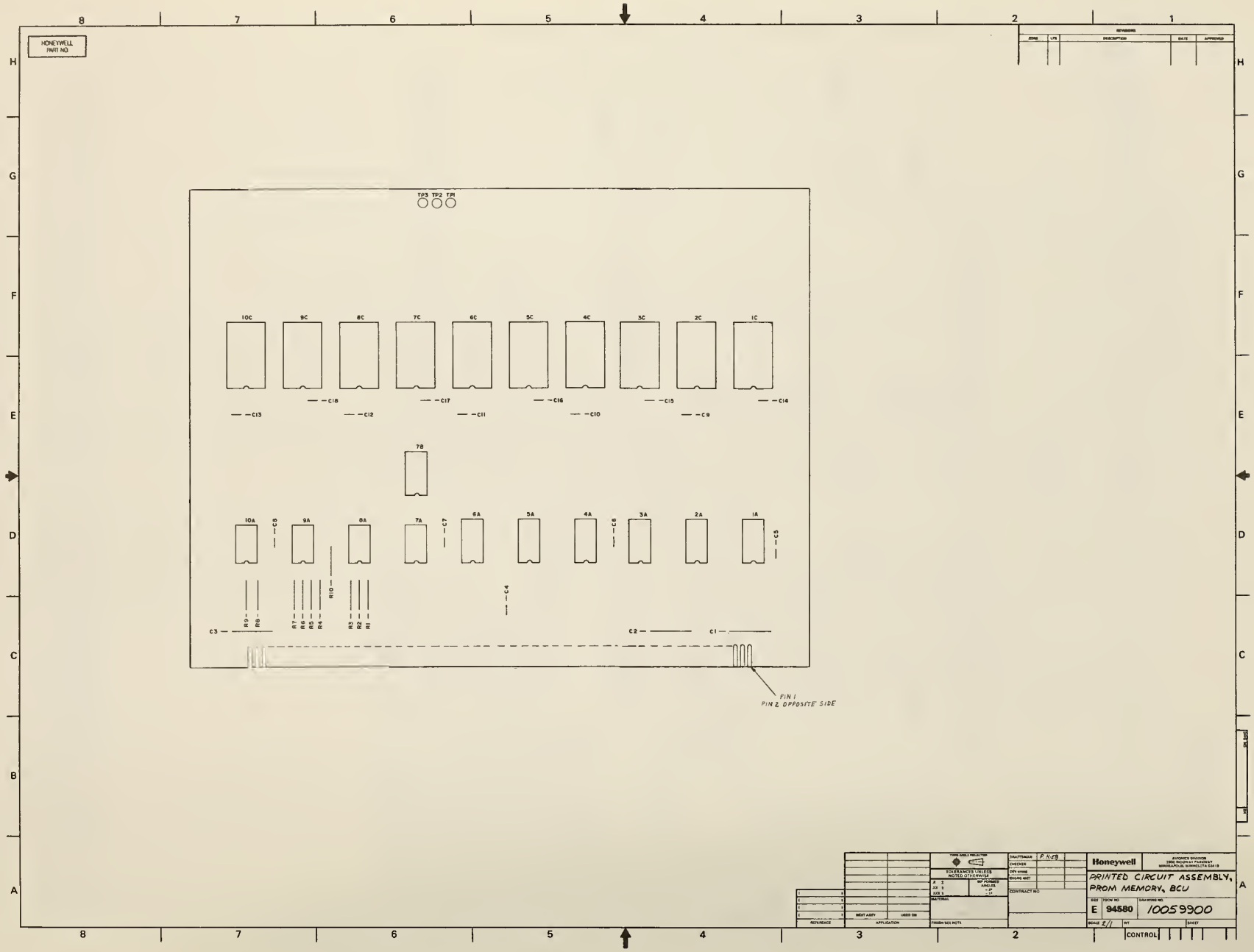
PL 10059900

TYPED BY	PPRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				1	1

PART NO.	PART NAME	QTY -101							
74LS367	BUS DRIVER, TRI-STATE	5	1A, 2A, 3A, 4A, 5A						
IM5623M	256x4 PROM	1	6A				Intersil		
74LS155	1 of 8 Decoder	1	8B						
MM5204	512x8 EPROM	6 △1					National Semi		
74LS00	QUAD NAND	1	7A						
74LS04	HEX INVERTER	1	8A						
7405	HEX INVERTING OC BUF	1	9A						
7437	QUAD NAND BUFFER	1	10A						
703-3790-01-04-16	Socket, IC, 24PIN	6 △1					Cambion		
TGS10	CAPACITOR, .01 µf	15	C4,5, 13,14,	6,7,8, 15,16,	9,10,11, 17,18	12,	Sprague		
M39003/01-2277	" , 150 µf	2	C1,3						
M39003/01-2301	CAPACITOR, 100µF	1	C2						
RCR07G102JP	RESISTOR 1K	6	R1,4,	5,6,	7,10				
RCR07G472JP	RESISTOR 4.7K	4	R2,3,	8,9					
448934-7	TERMINAL	2	TP1,	2	ALT: 15	12-2	CAMBION		
10063320	PC BOARD	1							

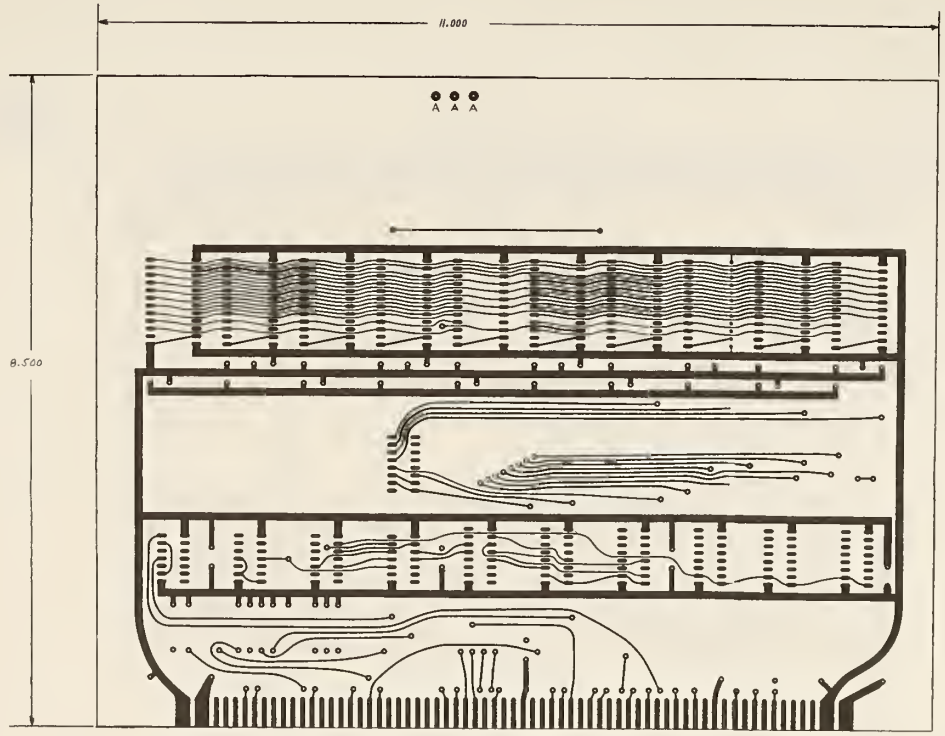
△1 - SEE SCHEMATIC FOR COMPONENT LOCATION AND COMPONENTS USED

HF-124


HONEYWELL PART NO.
TP3 TP2 TP1
10C 9C 8C 7C 6C 5C 4C 3C 2C 1C
C13 C18 C12 C17 C11 C16 C10 C15 C9 C14
7B
10A 9A 8A 7A 6A 5A 4A 3A 2A 1A
C8 C7 C6 C5
R10
R9 R8 R7 R6 R5 R4 R3 R2 R1
C4
C3 C2 C1
PIN 1
PIN 2 OPPOSITE SIDE
Honeywell
PRINTED CIRCUIT ASSEMBLY, PROM MEMORY, BCU
E 94580
10059900
CONTROL

HONEYWELL PART NO

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



HOLE CHART	
CODE	HOLE SIZE
NONE	.041
A	.070

7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.

6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS.

5 NUMBER INSIDE "O" INDICATES SIDE 1 AND 2 OF BOARD. LETTER INSIDE "O" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".

4 SHEETS 2, 3, 4 AND 5 ART DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCE PRINTED WIRING BOARD [illegible]. SHEETS 2 AND 3 ART ARTWORKS FOR SIDES 1 AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE 1 OF BOARD.

3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.

2 PARTS SHALL CONFORM TO ESI 901 EXCEPT AS NOTED ON THIS DRAWING.

1 MATERIAL MC8025-01, COPPER CLAD LAMINATE, .062 (REF) THICK, COPPER BOTH SIDES .0022 MIN THICK.

12 SHEET 4 ONLY SOLDER RESIST DATA:
- A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC-401 OR EQUIVALENT.
- B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
- C. SOLDER RESIST PATTERN ALIGNMENT TO BE [illegible] .010 DIA TO INDICATED FEATURES.
- D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 L .005 PER SIDE.

11 PATHWORK DIMENSIONAL DATA (REFERENCE):
- A. WIDTH OF CONDUCTIVE PATHS .015 MIN
- B. CLEARANCE BETWEEN CONDUCTIVE PATHS .015 MIN
- C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD .150 MIN.
- D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS .150 MIN.

10 ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.

9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.

8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF . MINIMUM.

16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00001-.150 MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.

15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.

14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).

13 SHEET 5 ONLY SILKSCREEN DATA.
- A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
- B. COLOR SHALL BE WHITE.
- C. SILKSCREEN PATTERN ALIGNMENT TO BE [illegible] .050 DIA TO INDICATED FEATURES.

TOLERANCES UNLESS NOTED OTHERWISE				
NEXT ASSY	USED ON			

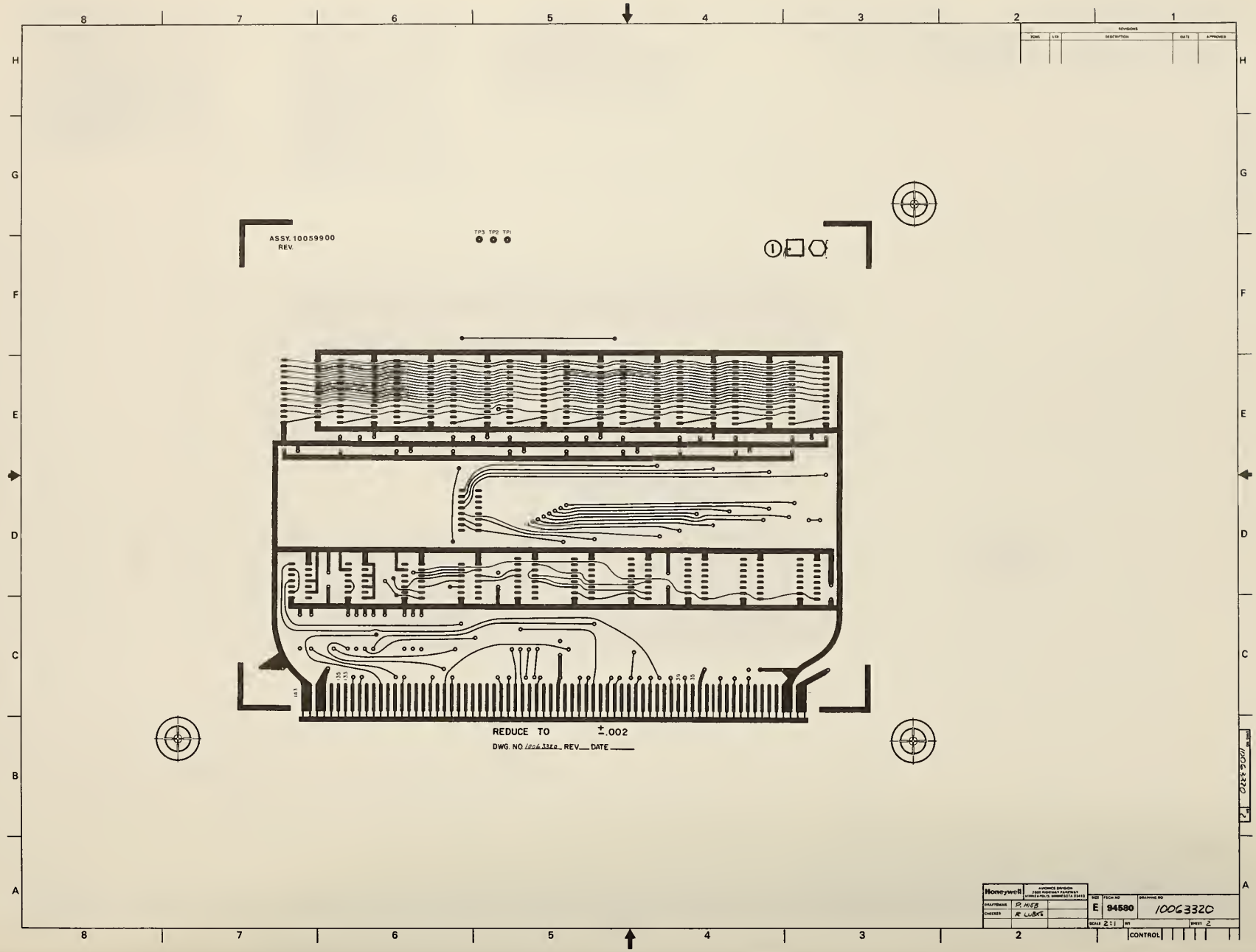
Honeywell

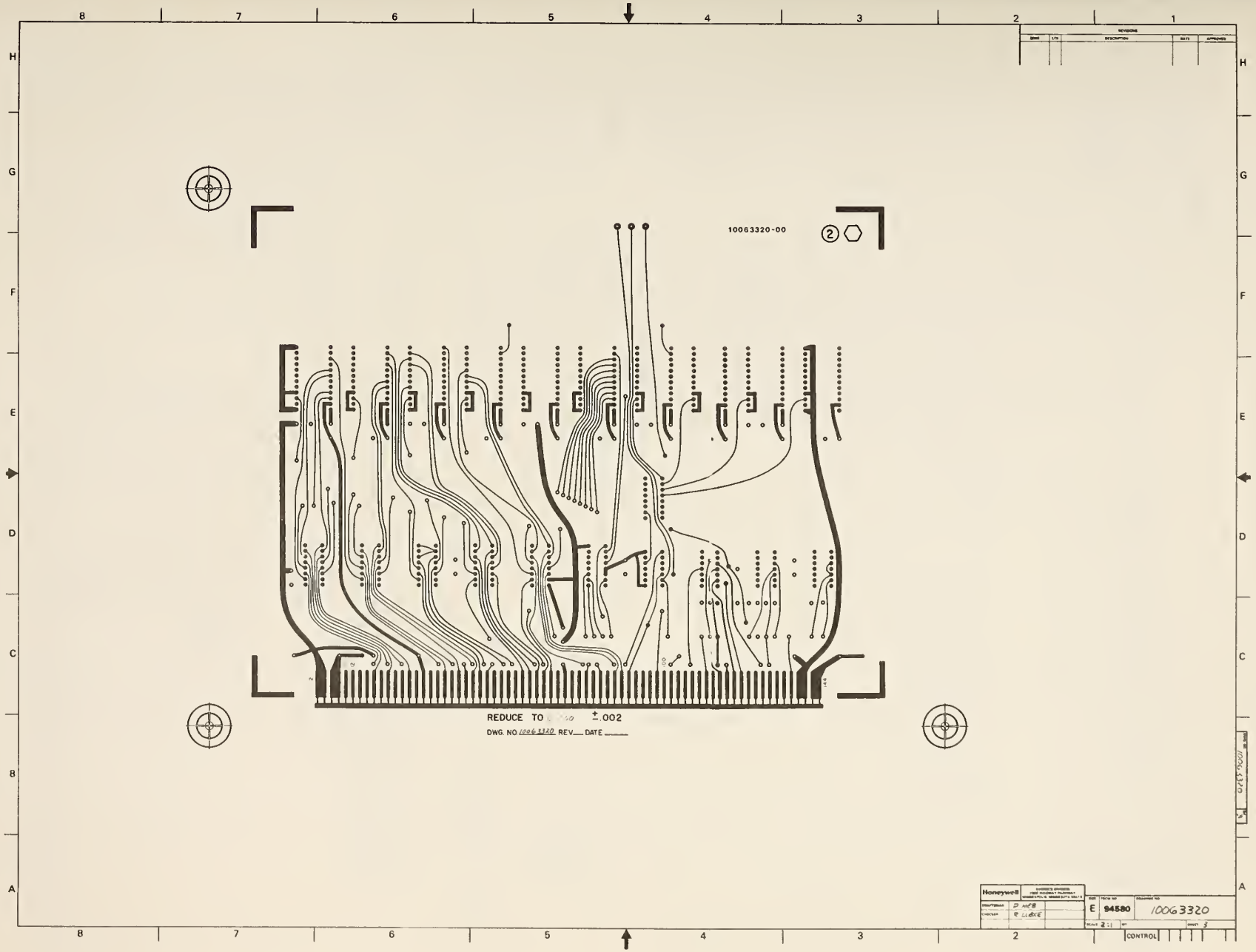
PRINTED CIRCUIT BOARD-
PROM MEMORY, BCU

SIZE	FSCM NO	DRAWING NO
E	94580	10063320

SCALE 2:1 WT SHEET 1

CONTROL


ASSY. 10059900
REV.
TP3 TP2 TP1
REDUCE TO ±.002
DWG. NO. 10063320 REV. DATE
Honeywell
DRAFTSMAN P. HIEB
CHECKER R. LUBKE
SIZE E
TECH NO 94580
DRAWING NO 10063320
SCALE 2:1
SHEET 2
CONTROL


10063320-00
2
REDUCE TO ±.002
DWG. NO 10063320 REV. DATE
Honeywell
D. WEB
R. LUBKE
E 94580
10063320
CONTROL

Honeywell

PRINTED IN U. S. A.

SUPERSEDES
SUPERSEDED BY

ENGINEERING PARTS LIST

REV.	DATE	E.O.	REV.	DATE	E.O.
	2Mar77				
A	6-9-77				

BUS DETECTOR, I/O — 10059899

TYPED BY	PRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				2	1

PART NO.	PART NAME	QTY							
74LS174	Hex D Register	6	1B, 2B, 3B, 4B, 5B, 6B						
7407	Hex OC Buffer	6	1A, 2A, 3A, 4A, 5A, 6A						
74LS00	Quad NAND	2	8A, 10A						
74LS74	DUAL D FLIP-FLOP	2	8D, 9A						
74LS221	DUAL MONOSTABLE F-F	2	6D, 7A						
74LS02	QUAD NOR	3	7D, 9B, 10C						
74LS04	HEX INVERTER	1	7B						
74LS138	1 OF 8 DECODER	2	8C, 9C						
7425	DUAL 4 NOR	1	8A						
7406	HEX OC INVERTER	1	9D						
CD4023	TRIPLE NAND	1	6C					RCA	
CD4009	HEX INVERTER	1	10D					RCA	
74LS27	TRIPLE 3 NOR	1	7C						
LM211D	COMPARATOR	1	4C				NATIONAL SEMI		
T8201	SWITCH SPDT	2	SW1, 3		CUTLER-HAMMER				
B8600	" SPST MOM	1	SW2		CUTLER-HAMMER				
RCR07G621JP	RESISTOR, 620Ω, ¼W	1	R10						
RCR07G243JP	" , 24K, "	1	R11						
RCR07G100JP	" , 10K, "	2	R1, 12						
RCR07G104JP	" , 100K, "	3	R13, 14, 18						
RCR07G393JP	" , 39K, "	1	R22						
RCR07G274JP	" , 270K, "	1	R16						
RCR07G514JP	" , 510K, "	1	R19						

HE-124

Honeywell

PRINTED IN U. S. A.

SUPERSEDES
SUPERSEDED BY

ENGINEERING PARTS LIST

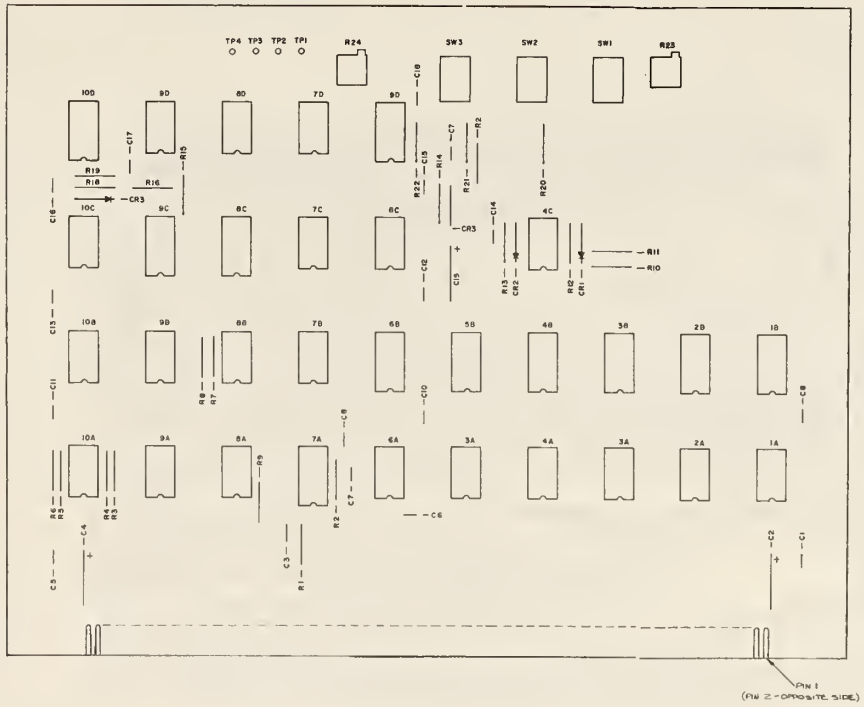
REV.	DATE	E.O.	REV.	DATE	E.O.
	29 Mar 77				
A	6-?-77				
B	7-27-77				
C	9-8-77				
D	10-6-77				

BUS DETECTOR, I/O — 10059899

TYPED BY	PRRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				2	2

PART NO.	PART NAME	QTY							
RCR07G472JP	RESISTOR, 4.7K 1/4W	4	R7,	8,	9,	20,	21		
3389H	POTENTIOMETER, 50K	1	R24					BOURNS	
3389H	" , 100K	1	R23					BOURNS	
RCR07G102JP	RESISTOR, 1K, 1/4 W	4	R3,	4,	5,	6			
1N914	DIODE	3	CR2,	3,	4				
1N821	DIODE, ZENER	1	CR1						
CK06BX105K	CAPACITOR, 1 μf	4	C8,	17,	18,	20			
CK05BX102K	" , .001	2	C7,	14					
TGS10	" , .01	10	C1,	5,	6,	9,	10, 11,	12, 13, 15, 16	SPRAGUE
CK05BX100K	" , 10pf	1	C3						
M39003/01-2295	" , 47 μf	1	C19				ALT: 10029798-169		
M39003/01-2277	" , 150 μf	2	C2, 4				ALT: 10029798-128		
74LS73	DUAL J-K FF	1	10B						
RCR07G822JP	RESISTOR, 82K	1	R2						
448934-7	TERMINAL	4	TP1,	2,	3,	4	ALT: 1512-2	CAMBION	
10063321	PC BOARD	1							

HC-124



HONEYWELL PART NO.

REVISIONS

SYMB	LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS NOTED OTHERWISE

DRAWN P. Ives

CHECKED

CONTRACT NO.

Honeywell

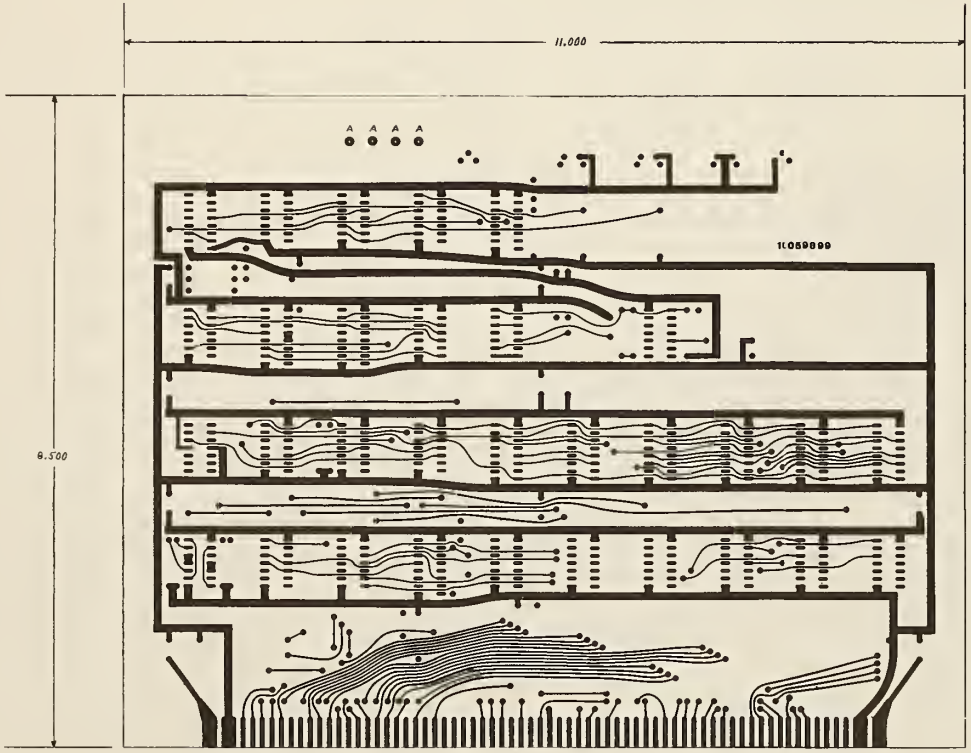
PRINTED CIRCUIT ASSEMBLY I/O, BCU

SIZE E | PROJ NO. 94880 | DRAWING NO. 10059899

SCALE 2/1 | SHT | SHEET

CONTROL

HONEYWELL PART NO



HOLE CHART	
CODE	HOLE SIZE
NONE	.041
A	.070

7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.

6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS [A | B | .005 DIA] UNLESS OTHERWISE SPECIFIED.

5 NUMBER INSIDE "⬡" INDICATES SIDE 1 AND 2 OF BOARD. LETTER INSIDE "⬡" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".

4 SHEETS 2, 3, 4 AND 5 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCE PRINTED WIRING BOARD 10063321. SHEETS 2 AND 3 ARE ARTWORKS FOR SIDES 1 AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE 1 OF BOARD.

3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.

2 PARTS SHALL CONFORM TO ES1301 EXCEPT AS NOTED ON THIS DRAWING.

1 MATERIAL MC8025-01, COPPER CLAD LAMINATE, .062 (REF) THICK, COPPER BOTH SIDES .0022 MIN THICK.

12 SHEET 4 ONLY SOLDER RESIST DATA:
- A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC401 OR EQUIVALENT.
- B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
- C. SOLDER RESIST PATTERN ALIGNMENT TO BE [⊕ .010 DIA] TO INDICATED FEATURES.
- D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 (.005 PER SIDE).

11 PATHWORK DIMENSIONAL DATA (REFERENCE):
- A. WIDTH OF CONDUCTIVE PATHS .015" MIN
- B. CLEARANCE BETWEEN CONDUCTIVE PATHS .015" MIN
- C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD .050 MIN.
- D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS .050 MIN.

10 ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.

9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.

8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF . MINIMUM.

16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00005 (50 MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.

15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.

14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).

13 SHEET 5 ONLY SILKSCREEN DATA:
- A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
- B. COLOR SHALL BE WHITE.
- C. SILKSCREEN PATTERN ALIGNMENT TO BE [⊕ .050 DIA] TO INDICATED FEATURES.

REFERENCE	NEXT ASSY	USED ON

APPLICATION

THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE
X ± .1
.XX ± .01
.XXX ± .005
SQ FORMED AREA .125 ± .25

MATERIAL

FINISH SEE NOTE

DRAFTSMAN H. JOHNSON
CHECKER
APV ENGR
ENGRG MGT
CONTRACT NO

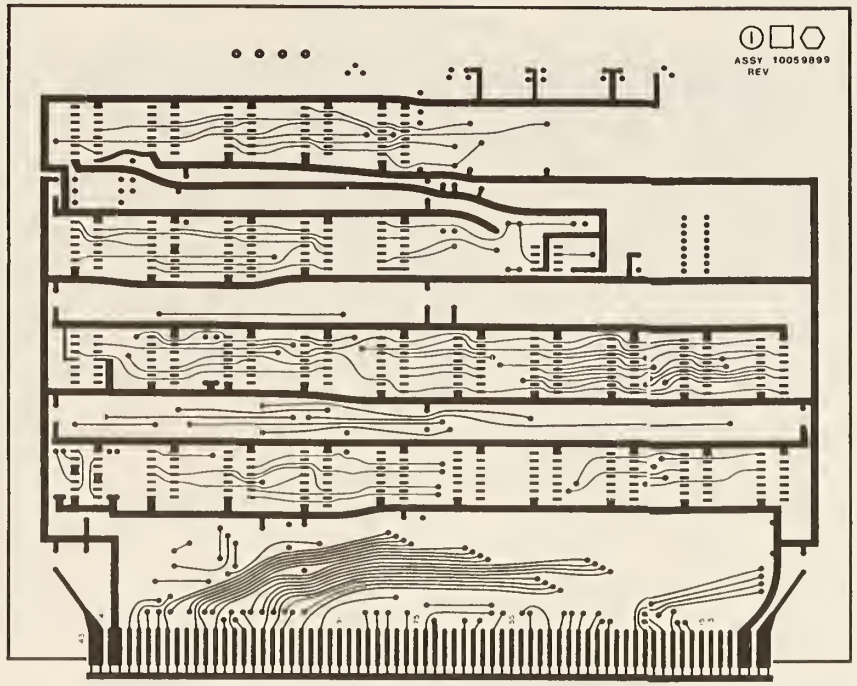
Honeywell
AVIONICS DIVISION
2600 RIDGEWAY PARKWAY
MINNEAPOLIS, MINNESOTA 55413

PRINTED CIRCUIT BOARD-I/O

SIZE E | FSCM NO 94580 | DRAWING NO 10063321

SCALE 2:1 | WT | SHEET 1

CONTROL



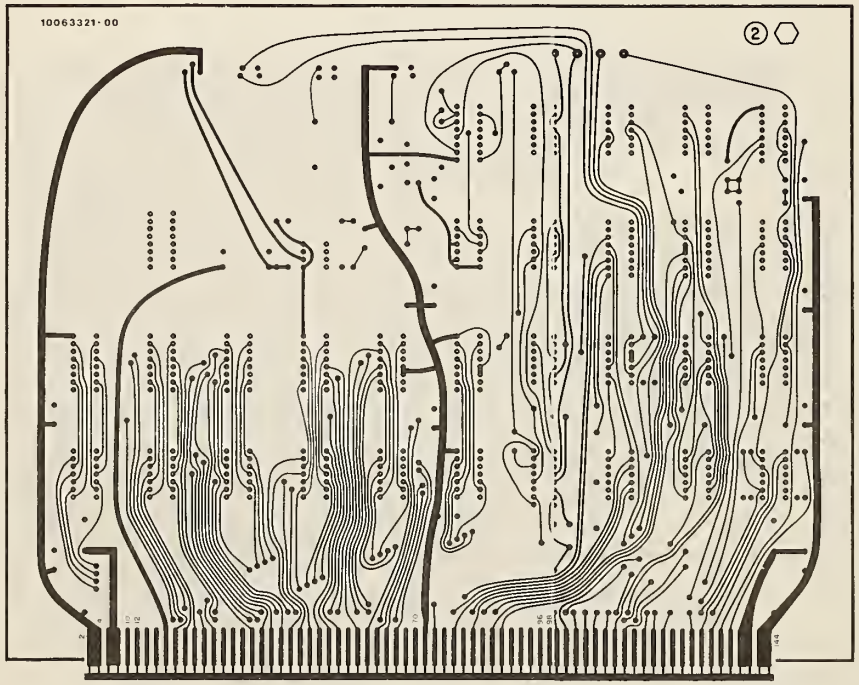
REDUCE TO ±.002

DWG NO 10063321 REV ___ DATE ___

Honeywell

E 94580 10063321

CONTROL



REDUCE TO ±.002

DWG. NO 10063321 REV___ DATE _____

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

Honeywell — AVIONICS DIVISION, 1200 NORTHEAST FAIRPORT, MINNEAPOLIS, MINNESOTA 55413

DRAFTSMAN: P. HEB

CHECKER: R. LUBKE

SIZE: E | FSCM NO: 94580 | DRAWING NO: 10063321

SCALE: 2:1 | WT | SHEET 3

CONTROL

Honeywell

PRINTED IN U. S. A.

SUPERSEDES
SUPERSEDED BY

ENGINEERING PARTS LIST

REV.	DATE	E.O.	REV.	DATE	E.O.
A	6-10-77				
B	7-28-77				

P.P. CONTROL DECODING CARD 1

10059904

TYPED BY	PRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				2	1

PART NO.	PART NAME	QTY							
7400	QUAD 2 NAND	1	2F						
74LS00	QUAD 2 NAND	3	4E,	9D,	11E				
74LS02	QUAD 2 NOR	3	1D,	9F,	11D				
7404	HEX INVERTER	1	5D						
74LS04	HEX INVERTER	6	1E,	2C,	7C,	7D,	8C,	10E	
7406	HEX OC INV	1	4F						
74LS08	QUAD 2 AND	2	2E,	7E					
74LS10	TRIPLE 3 NAND	1	6D						
74LS11	TRIPLE 3 AND	1	2D						
74LS27	TRIPLE 3 NOR	1	8F						
74LS30	8 NAND	1	8D						
74S140	DUAL 4 IN POS NAND	1	1F						
74LS37	QUAD 2 BUF NAND	1	9E						
74LS74	DUAL D FF	3	3F,	3E,	8E				
74LS138	3 TO 8 DECODER	3	2A,	6C,	9C				
74LS154	4 TO 16 DEC/DEM	2	3A,	4A					
74LS163	SYNC 4-BIT COUNT	2	5E,	6E					
74LS174	HEX QUAD D-FF	4	5A,	6A,	10A,	11A			
74LS175	HEX QUAD D-FF	3	3D,	4D,	10F				
74LS181	ALU	3	7A,	8A,	9A				
74LS194	4-BIT SHIFT REG.	2	1B,	1C,					
74LS197	BIN COUNTER/LATCH	2	3C,	4C,					
74LS251	DATA SEL/MULTIPLEX	1	11F						
74LS367	HEX BUS DRIVERS	5	5B,	5C,	10C,	11B,	11C		

HE-124

Honeywell

PRINTED IN U. S. A.

ENGINEERING PARTS LIST

SUPERSEDES
SUPERSEDED BY

REV.	DATE	E.D.	REV.	DATE	E.D.
A	6-10-77				
B	7-28-77				
C	9-8-77				
D	10-6-77				

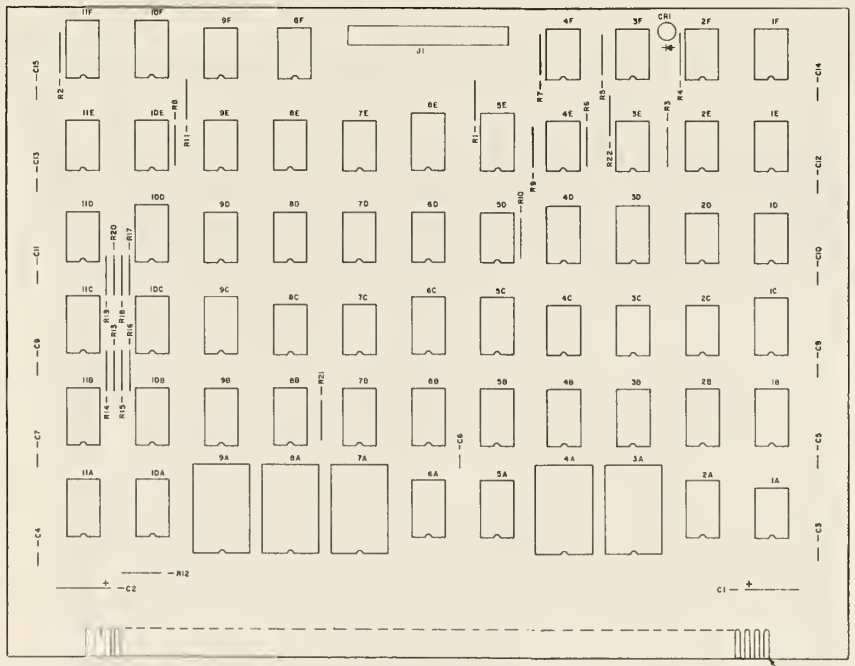
P.P. CONTROL DECODING CARD 1

10059904

TYPED BY	PPRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				2	2

PART NO.	PART NAME	QTY							
IM5623C	PROM	3	2B,	3B,	4B		INTERSIL		
DM8542	QUAD REG.	3	7B,	8B,	9B		National Semi		
DM8553	8-Bit Latch	2	6B,	10B			National Semi		
RCR07G102JP	RESISTOR 1K, ¼W	8	R3,	9,10,	11,12,	21,22,	23		
RCR07G151JP	RESISTOR 150, ¼W	2	R4,	7					
RCR07G472JP	RESISTOR 4.7K, ¼W	13	R2,5, 25	6,8,	13,14,	15,16,	17,18,	19,20,	24,
TG510	CAPACITOR .01	AR	C				SPRAGUE		
76B04 SPST	SWITCH (DIP)	2	T-SW	E-SW			Grayhill		
M39003/01-2277	CAPACITOR 150μF	2	C1,2		ALT: 10029798-128				
3432-1002	CONNECTOR	1						3M	
OSL-3L	LED	1	CR1					OPCOA	
K1100A	5MHz OSC	1	1A				MOTOROLA		
10063322	PC BOARD	1							

HE-124



HONEYWELL PART NO

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS NOTED OTHERWISE

Honeywell

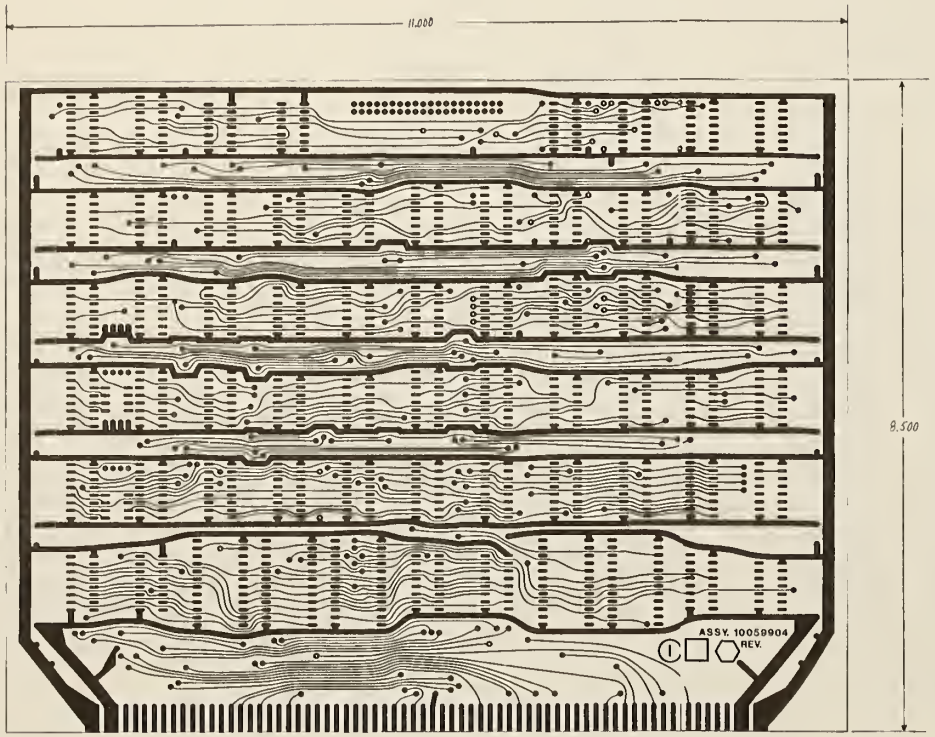
PRINTED CIRCUIT ASSEMBLY
PREPROCESSOR #1, BCU

SIZE E | CODE IDENT NO 94580 | DRAWING NO 10057704

SCALE 2/1 | SHEET

CONTROL

HONEYWELL PART NO



HOLE CHART	
CODE	HOLE SIZE
NONE	.041

7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.

6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS $\boxed{A \mid B \mid .005 \text{ DIA}}$ UNLESS OTHERWISE SPECIFIED.

5 NUMBER INSIDE "○" INDICATES SIDE 1 AND 2 OF BOARD. LETTER INSIDE "○" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".

4 SHEETS 2, 3, 4 AND 5 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCED PRINTED WIRING BOARD 10063322. SHEETS 2 AND 3 ARE ARTWORKS FOR SIDES 1 AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE 1 OF BOARD.

3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.

2 PARTS SHALL CONFORM TO ES1301 EXCEPT AS NOTED ON THIS DRAWING.

1 MATERIAL: MC8025-01, COPPER CLAD LAMINATE, .062 (REF) THICK, COPPER BOTH SIDES .0022 MIN THICK.

12 SHEET 4 ONLY SOLDER RESIST DATA:
- A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC8RE OR EQUIVALENT.
- B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
- C. SOLDER RESIST PATTERN ALIGNMENT TO BE $\boxed{\odot \mid .010 \text{ DIA}}$ TO INDICATED FEATURES.
- D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 (.005 PER SIDE).

11 PATHWORK DIMENSIONAL DATA (REFERENCE):
- A. WIDTH OF CONDUCTIVE PATHS .015 MIN
- B. CLEARANCE BETWEEN CONDUCTIVE PATHS .015 MIN
- C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD .150 MIN.
- D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS .150 MIN.

10 ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.

9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.

8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF . MINIMUM.

16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00005 (50 MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.

15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.

14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).

15 SHEET 5 ONLY SILKSCREEN DATA:
- A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
- B. COLOR SHALL BE WHITE.
- C. SILKSCREEN PATTERN ALIGNMENT TO BE $\boxed{\odot \mid .050 \text{ DIA}}$ TO INDICATED FEATURES.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

REFERENCE	NEXT ASSY	USED ON
APPLICATION		

TOLERANCES UNLESS NOTED OTHERWISE
DIMENSIONS ARE IN INCHES
MATERIAL
FINISH SEE NOTE

DRAFTSMAN
CHECKER
DES ENGR
ENGRG MGR
CONTRACT NO

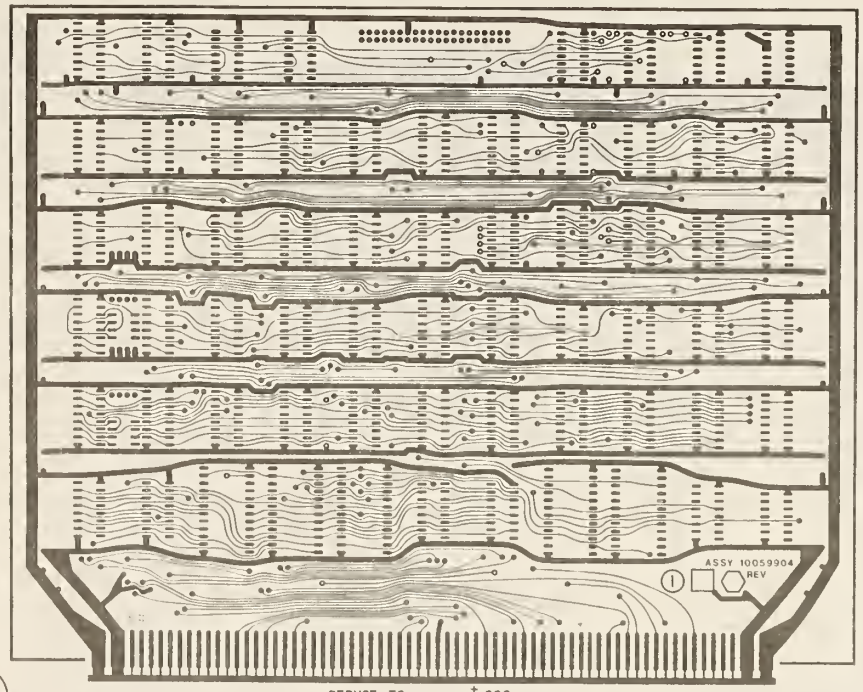
Honeywell
A HONEYWELL DIVISION
2600 RIDGEWAY AVENUE
MINNEAPOLIS, MINNESOTA 55413

PRINTED CIRCUIT BOARD
PREPROCESSOR #1, BCU

SIZE E | ITEM NO 94580 | DRAWING NO 10063322

SCALE 2/1 | WT | SHEET 1

CONTROL



REDUCE TO ±.002

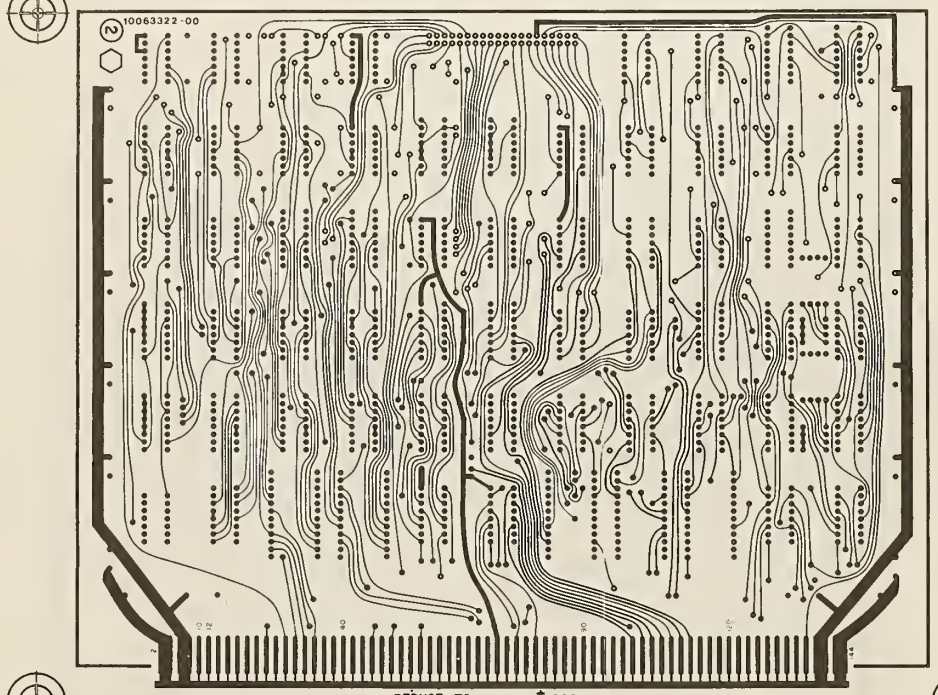
DWG NO 10063322 REV ___ DATE ___

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

Honeywell

E 94580 10063322

CONTROL



REDUCE TO [illegible] ±.002

DWG. NO. 10063322 REV. ___ DATE ___

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

Honeywell — AVIONICS DIVISION, 1000 FIDDLER PARKWAY, MINNEAPOLIS, MINNESOTA 55413

DRAFTSMAN	P. HEEB	SIZE E	FSCM NO 94580
CHECKER	R. LUEKE	DRAWING NO 10063322	
SCALE 2:1	WT	SHEET 3	

CONTROL

10063322 REV

Honeywell

PRINTED IN U. S. A.

SUPERSEDES
SUPERSEDED BY

REV.	DATE	E.O.	REV.	DATE	E.D.
A	7-12-77				
B	7-21-77				
C	10-6-77				

ENGINEERING PARTS LIST

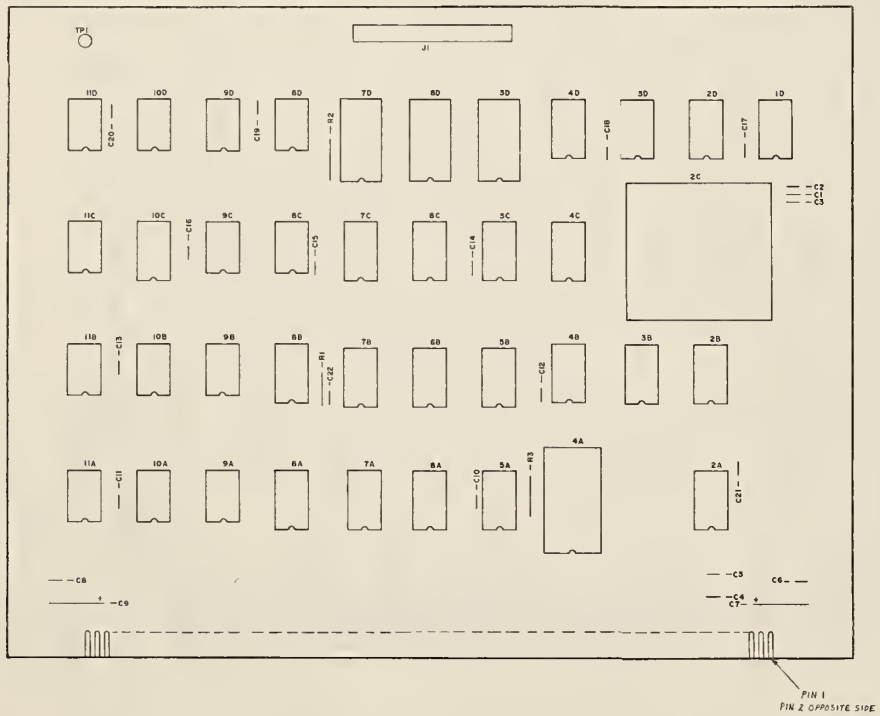
CYCLE STEAL CONTROL/ADDRESS PREPROCESSOR CARD 2

10059901

TYPED BY	PPRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				1	1

PART NO.	PART NAME	QTY							
74LS00	QUAD 2 NAND	1	9D						
74LS02	QUAD 2 NOR	3	10B,	8C,	8D				
74S04	HEX INVERTER	1	11A						
74LS04	HEX INVERTER	2	10A,	9C					
74LS08	QUAD 2 AND	1	11C						
74LS27	TRIPLE 3 NOR	1	9A						
7437	QUAD 2 BUF NAND	1	11B						
74LS74	DUAL D FF	2	11D,	9B					
74LS157	QUAD 2 MULT	1	5C						
74LS164	8BIT SHIFT REG.	1	10D						
74LS174	HEX QUAD D-FF	4	8B,	6B,	5B,	2B			
74LS193	4BT UP/DN COUNTER	2	7C,	4B					
74LS367	HEX BUS DRIVERS	14	10C,8A,	7A,7B,	6A,6C,	5A,4C	4D,2A,	3B,3D	2D,1D
2101A	256x4 RAM	3	7D,	6D,	5D		INTEL		
IH5060	16-Channel MUX	1	4A				INTERSIL		
ADC-EH8B1	A/D Converter	1	2C				DATEL		
RCR07G102JP	RESISTOR, 1K, 1/4W	3	R1,2,3						
TGS10	CAPACITOR, .01μF	14	C8	THRU	21		SPRAGUE		
CK06BX104K	CAPACITOR, .1μF	5	C1,2,3,4,5						
M39003/01-2277	CAPACTOR, 150μF	2	C6,7			ALT: 10029798-128			
3432-1002	CONNECTOR	1						3M	
10063323	PC BOARD	1							

HE-124



HONEYWELL PART NO

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

DRAFTSMAN	R.H.E.B.	Honeywell	AVIONICS DIVISION 2600 RIDGEWAY PARKWAY MINNEAPOLIS, MINNESOTA 55413
CHECKER		PRINTED CIRCUIT ASSEMBLY, PREPROCESSOR #2, BCU	
DEV ENGR			
ENGRG MGT			
CONTRACT NO.		SIZE E / FSCM NO. 94580	DRAWING NO. 10059901
		SCALE 2/1	WT. / SHEET
		CONTROL	

TOLERANCES UNLESS NOTED OTHERWISE

MATERIAL

FINISH-SEE NOTE

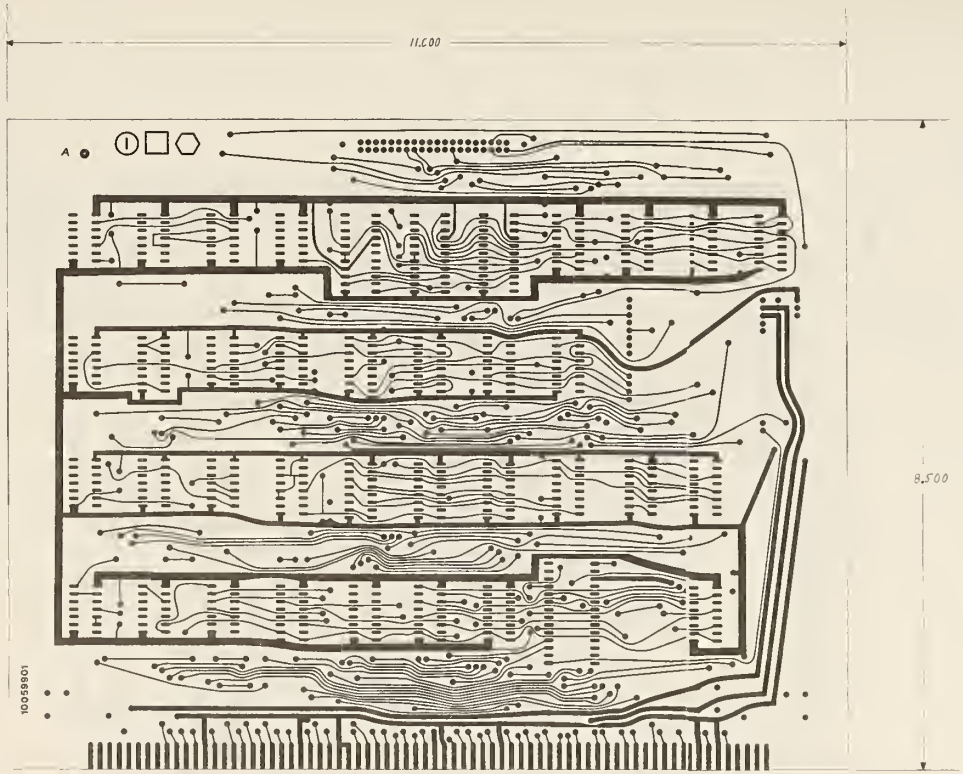
NEXT ASSY / USED ON

APPLICATION

DEPENDENCY

HONEYWELL PART NO

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



HOLE CHART	
CODE	HOLE SIZE
NONE	.041
A	.070

7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.

6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS. [B] .005 DIA] UNLESS OTHERWISE SPECIFIED.

5 NUMBER INSIDE "O" INDICATES SIDE E AND 2 OF BOARD. LETTER INSIDE "O" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".

4 SHEETS 2, 3, 4 AND 5 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCE PRINTED WIRING BOARD (MASTER). SHEETS 2 AND 3 ARE ARTWORKS FOR SIDES E AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE E OF BOARD.

3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.

2 PARTS SHALL CONFORM TO ESTRE EXCEPT AS NOTED ON THIS DRAWING.

1 MATERIAL: MC0025-01, COPPER CLAD LAMINATE, .062 (REF) THICK. COPPER BOTH SIDES .0022 MIN THICK.

12 SHEET 4 ONLY SOLDER RESIST DATA
- A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC-401 OR EQUIVALENT.
- B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
- C. SOLDER RESIST PATTERN ALIGNMENT TO BE [B] .010 DIA TO INDICATED FEATURES.
- D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 (.005 PER SIDE).

11 PATHWORK DIMENSIONAL DATA (REFERENCE):
- A. WIDTH OF CONDUCTIVE PATHS .005" MIN
- B. CLEARANCE BETWEEN CONDUCTIVE PATHS .015" MIN
- C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD .120 MIN.
- D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS .020 MIN.

10 ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.

9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.

8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF . MINIMUM.

16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00005 (50 MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.

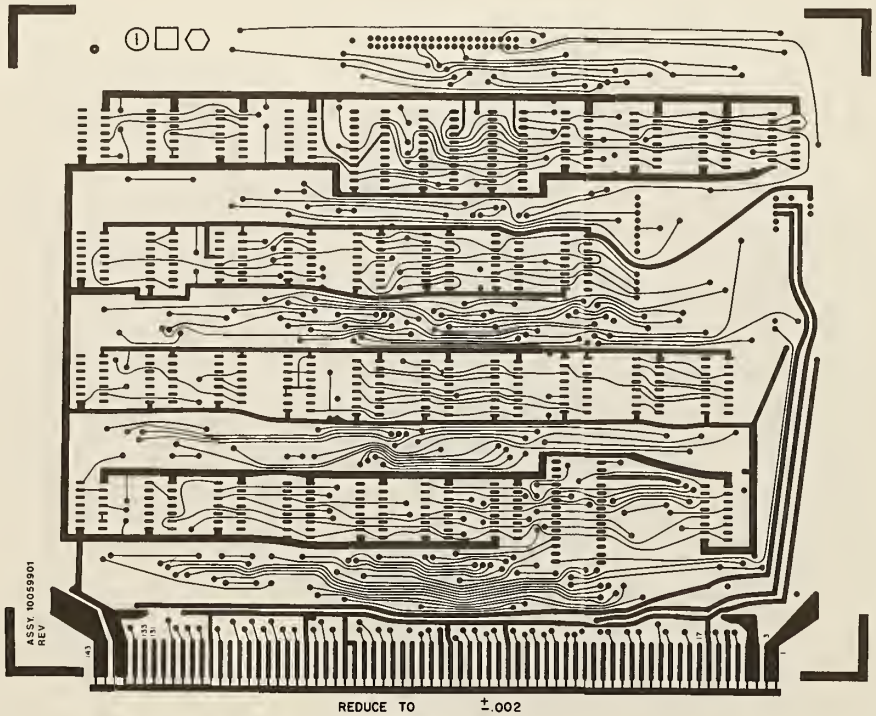
15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.

14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).

13 SHEET 5 ONLY SILKSCREEN DATA
- A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
- B. COLOR SHALL BE WHITE.
- C. SILKSCREEN PATTERN ALIGNMENT TO BE [B] .090 DIA TO INDICATED FEATURES.

TOLERANCES UNLESS NOTED OTHERWISE	DRAFTSMAN	Honeywell	
	TOOL NO		
	DES SPEC		
	PROJECT NO		
	CONTRACT NO	PRINTED CIRCUIT BOARD PREPROCESSOR #2	
		SIZE E	DRAWING NO 10063323
		SCALE 4	SHEET 1

CONTROL

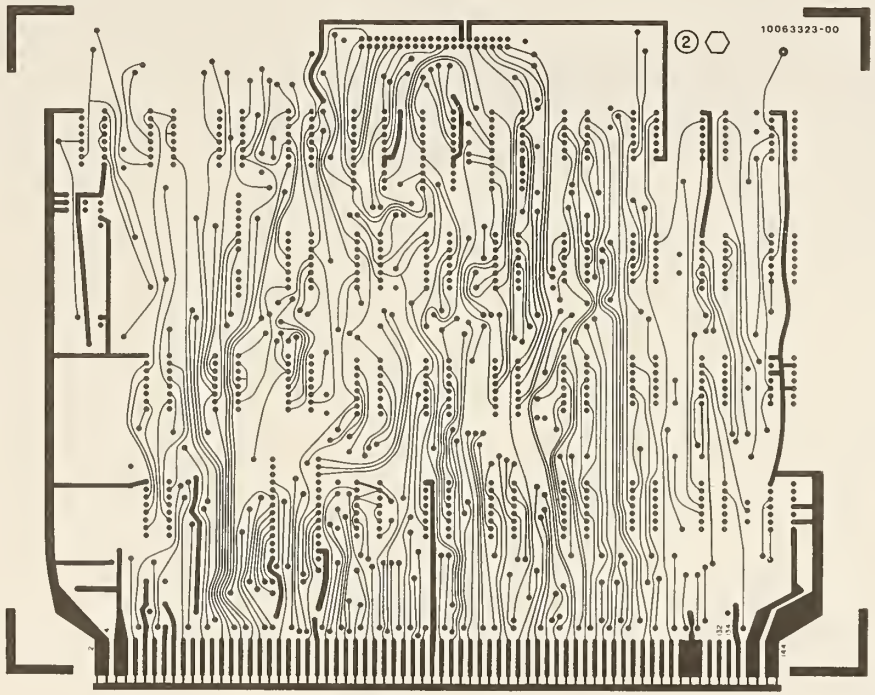


REDUCE TO ±.002

DWG. NO 10063323 REV___ DATE___

Honeywell	AVIONICS DIVISION 2600 RIDGEWAY PARKWAY MINNEAPOLIS, MINNESOTA 55413	SIZE E	FSCM NO 94580	DRAWING NO 10063323	
DRAFTSMAN D. HEB		SCALE 2:1	WT	SHEET 2	
CHECKER R. LUBKE					

CONTROL



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

Honeywell

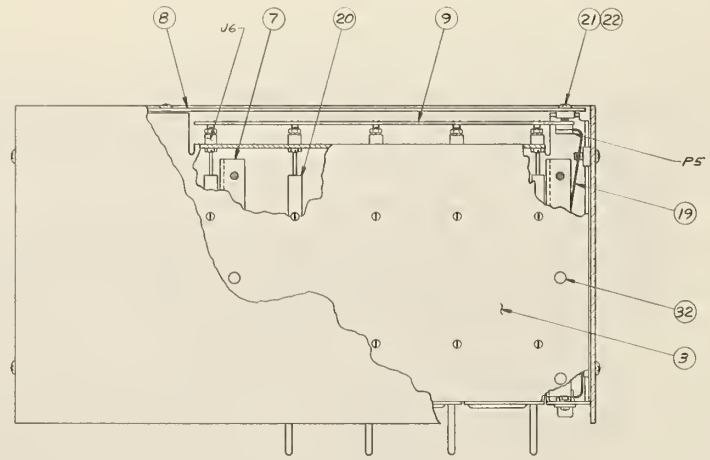
DRAFTSMAN P. KEB
CHECKER R. LUBKE

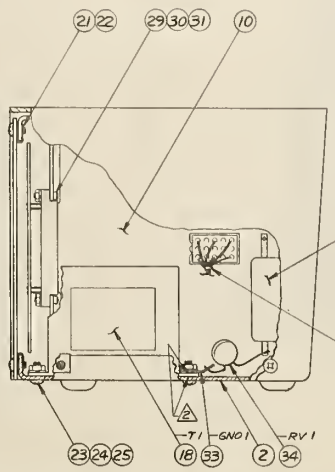
PROJ NO E 94580
DRAWING NO 10063323
SCALE 2:1 SHEET 3

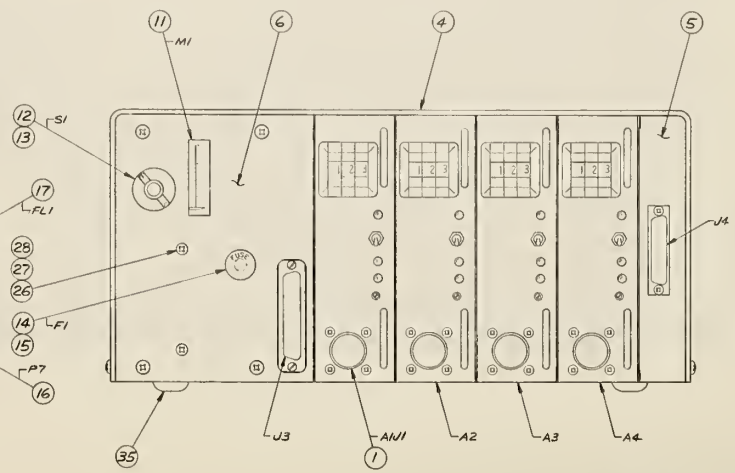
CONTROL

DASH NO. -001

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	R/V	8-5-77	







QTY	PART NO.	DESCRIPTION	MATERIAL OR SPECIFICATION		ITEM NO.
4	SJ5123	BUMPER	3M		35
1	V150LA10	VARISTOR	RV1	G.E.	34
1		LUG, GROUND	NO.8	GND 1	33
12	AAP-52	RIVET, POP		CHERRY	32
10		NUT, HEX	4-40		31
10		LOCKWASHER, SPLIT	NO.4		30
10		SCREW, PAN HEAD	4-40 x .50LG		29
2		NUT, HEX	6-32		28
2		LOCKWASHER	NO 6		27
2		SCREW, PAN HEAD	6-32 x .38 LG		26
2		NUT, HEX	8-32		25
2		LOCKWASHER	NO.8		24
2		SCREW, PAN HEAD	8-32 x .38LG		23
14		SCREW	8A or 8Z x .38LG		22
14	C11539-8-4	NUT, CLIP		TINNERMAN	21
10	1450F	CARD GUIDE		S.A.E.	20
1	28021590-001	CABLE ASSY, SIGNAL			19
1	F-54X	TRANSFORMER	T1	TRIAD-UTRAD	18
1	1R1	FILTER, RFI LINE	FL1	CORCOM	17
1	28021589-001	CABLE ASSY, POWER SUPPLY			16
1	HLF	FUSEHOLDER		BUSSMAN	15
1		FUSE, 1 AMP	F1		14
1	5-11731-427	SWITCH, ROTARY	S1	OAK	13
1	SS-50BLTS-2	KNOB		BUCKEYE	12
1	MODEL 1921	METER, VERTICAL 0-10VDC	M1	SIMPSON	11
1	10059902-101	PWB ASSY, RELAY & PWR SUPPLY			10
1	10063313-101	PWB ASSY, MOTHER			9
1	28021586-001	COVER, REAR			8
1	28021585-001	BRACKET, SHIELD			7
1	28021587-001	PANEL, FRONT			6
1	28021584-001	BRACKET, SHIELD			5
1	28021588-001	COVER, TOP			4
1	28021583-001	CHASSIS, TOP			3
1	28021582-001	CHASSIS, BOTTOM			2
4	10059903-101	PWB ASSY, LOOP ELECTRONICS	A1-A4		1

2 REMOVE PAINT BEFORE ASSEMBLING
1 - FOR MATING CABLE SEE 28021596 AND 28021592
BUS CLASSIFIER ASSY SEE 28021574
BCU TO LOOP DETECTOR CABLE SEE 28021595
LOOP ELECTRONICS EXTENDER BOARD SEE 10063311

LOOP DET

DRAWN BY R.W. Ruhlen 4-26-77

HONEYWELL INC. — TRAFFIC MANAGEMENT CENTER

LOOP DETECTOR ASSEMBLY

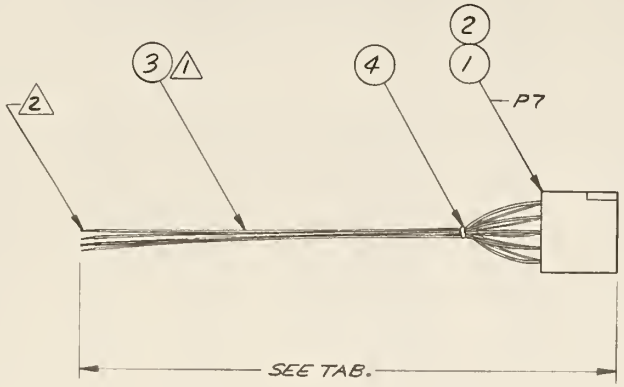
SIZE F — DWG NO. 28021581 — SCALE 1/1 — SHEET 1 OF

CONTROL

DASH NO. -001

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

P7 PIN	LENGTH	WIRE SIZE 1
1	7.0 ± .5	16 AWG
2		
3		
4		
5		
6		
7		22 AWG
8		
9		
10		
11		
12	NO WIRE	
13		
14		
15		



QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	REMARKS	ITEM NO
1	TY-23M	CABLE TIE	T & B	4
AR	1	LEADWIRE		3
11	02-09-1134	CONTACT, FEMALE	MOLEX	2
1	03-09-1152	CONNECTOR, RECEPTACLE	P7 MOLEX	1

2 STRIP INSULATION 3/8 INCH AND TIN

1 ALL LEADWIRE MIN 19 STRANDS PER MIL-W-16878D, TYPE B OR D, 600V, 105°C, VINYL NYLON JACKET OR IRRATIATED CROSS LINKED PVC. SIZE PER TAB.

REFERENCE	NEXT ASSY	USED ON
	28021581	LOOP DET

-001 THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE: X ±, XX ±, XXX ±; 90° FORMED ANGLES -1° +2°

MATERIAL

FINISH – SEE NOTE

DRAWN BY J. Pearson 4-22-77; CHECKER; DEV ENGR; ENGRG MGT

CONTRACT NO

AGENCY APPROVAL

HONEYWELL INC — TRAFFIC MANAGEMENT CENTER

CABLE ASSY, PWR SUPPLY

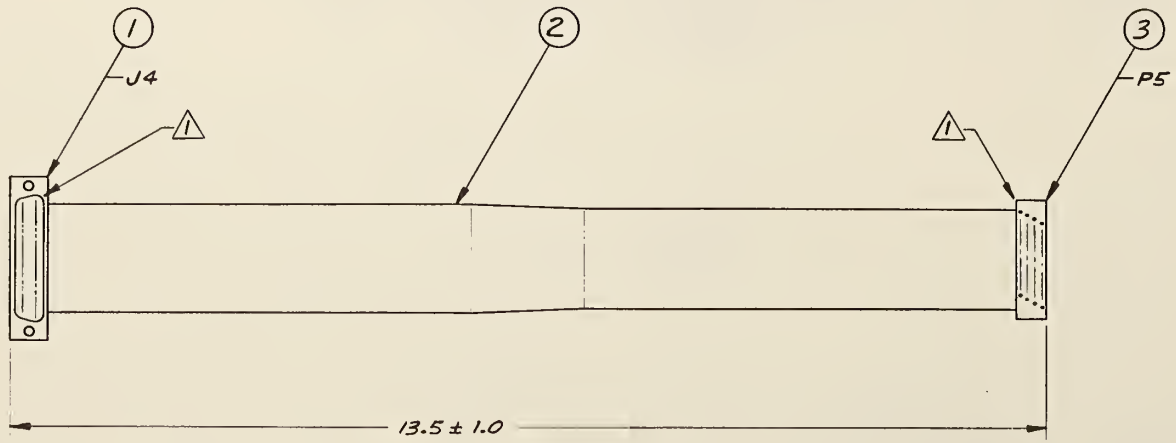
SIZE C; FSCM NO; DWG NO 28021589; SCALE 1/1; SHEET 1 OF

CONTROL

TMC C 1/77

DASH NO. -001

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	REV	8-5-77	



QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	REMARKS	ITEM NO
1	3434-0000T	CONNECTOR, PCB	P5 3M	3
AR	3349/25	CABLE, FLAT	3M	2
1	3482-1000	CONNECOR, DELTA	J4 3M	1

REFERENCE	NEXT ASSY	USED ON
( )		
( )		
( )		
( )		
( )	28021581	LOOP DET

-001 THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE: X ±, XX ±, XXX ±; 90° FORMED ANGLES ±1° +2°

MATERIAL

FINISH—SEE NOTE

DRAWN BY A.H. Johnson 4-20-77; CHECKER; DEV ENGR; ENGRG MGT; CONTRACT NO; AGENCY APPROVAL

HONEYWELL INC — TRAFFIC MANAGEMENT CENTER

CABLE ASSY, SIGNAL

SIZE C; FSCM NO; DWG NO 28021590; SCALE 1/1; SHEET 1 OF

CONTROL

△1 - PIN 1 THIS END

TMC-C 1/77

Honeywell

PRINTED IN U. S. A.

SUPERSEDES
SUPERSEDED BY

ENGINEERING PARTS LIST

REV.	DATE	E.O.	REV.	DATE	E.O.
A	10-10-77				
B	10-13-77				

LOOP ELECTRONICS — 10059903

TYPED BY	PRRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				3	1

PART NO.	PART NAME	QTY							
28021593-001	PANEL, FRONT	1							
T65F-02M	"F" POST BCD THUMBWHEEL	3	S1,2,3					CHERRY	
T60	END CAP, THUMBWHEEL SW	2						CHERRY	
7211A	SWITCH, TOGGLE	1	S4					C&K	
OSL-3L	LED	3	CR1,2,3						
3009P-1-503	POTENTIOMETER 50K	1	R12					BOURNS	
415-1230-01-18	HANDLE	2						CAMBRIDGE	
1-380949-2	RECEPTACLE ASSY	3						AMP	
MS3102 -14S-7P	CONNECTOR	1	J1						
CD4013	"D" FF	1	U2						
CD4030	EXC OR	1	U4						
CD4049	HEX INVERTER	1	U3						
CA3100	OP AMP	1	U6						
CA3130	OP AMP	1	U5						
74C221	MONO MULTIVIBRATOR	1	U1						
2N2222	TRANSISTOR	3	Q1,2,3						
1N5357	DIODE, ZENER, 20V	2	CR4,5						
200 KHZ	CRYSTAL	1	Y1						
RCR07G511JP	RESISTOR, 510	2	R25,26						
RCR07G103JP	RESISTOR, 10K	4	R3, 7, 19, 22						
RCR07G153JP	RESISTOR, 15K	1	R11						

HE-124

Honeywell

PRINTED IN U. S. A.

SUPERSEDES
SUPERSEDED BY

ENGINEERING PARTS LIST

LOOP ELECTRONICS

10059903

REV.	DATE	E.O.	REV.	DATE	E.O.
A	9-2-77				

TYPED BY	PPRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				3	2

PART NO.	PART NAME	QTY							
RCR07G203JP	RESISTOR, 20K	1	R17						
RCR07G273JP	RESISTOR, 27K	2	R20,	21					
RCR07G333JP	RESISTOR, 33K	1	R13						
RCR07G822JP	RESISTOR, 8.2K	1	R29						
RCR07G104JP	RESISTOR, 100K	3	R16,	23,	24				
RCR07G154JP	RESISTOR, 150K	2	R27,	28					
RCR07G204JP	RESISTOR, 200K	1	R10						
RCR07G334JP	RESISTOR, 330K	1	R14						
RCR07G105JP	RESISTOR, 1MEG	3	R5,	6,	9				
RCR07G512JP	RESISTOR, 5.1K	2	R1,	2					
RW70U1001	RESISTOR, 1K	3	R4,	8,	15				
RT24C2P103	TRIMPOT, 10K	1	R18						
NE2	LAMP, NEON	1	DS1	(CR6)					
DIT270	TRANSFORMER	1	T1						UTC
8000-DG3	CRYSTAL HOLDER	1							AUGAT
CK05BX332K	CAPACITOR .0033	1	C3						
TGS10	CAPACITOR .01	3	C6,	8,	12				DISC
CK05BX153K	CAPACITOR .015	1	C4						
CK05BX104K	CAPACITOR .1	3	C1,	9,	10			CERAMIC	
CK06BX334K	CAPACITOR .33	1	C5						
M39003/01-2365	CAPACITOR 3.3	1	C2						
M39003/01-2301	CAPACITOR 100	1	C11						20V
SX420	CAPACITOR 20pF	1	C1	POLYSTYRENE-MALLORY					
SX439	CAPACITOR 39pF	1	C2						

HE-124

Honeywell

PRINTED IN U. S. A.

ENGINEERING PARTS LIST

SUPERSEDES / SUPERSEDED BY					
REV.	DATE	E.O.	REV.	DATE	E.O.
A	9-1-77				
B	10-6-77				

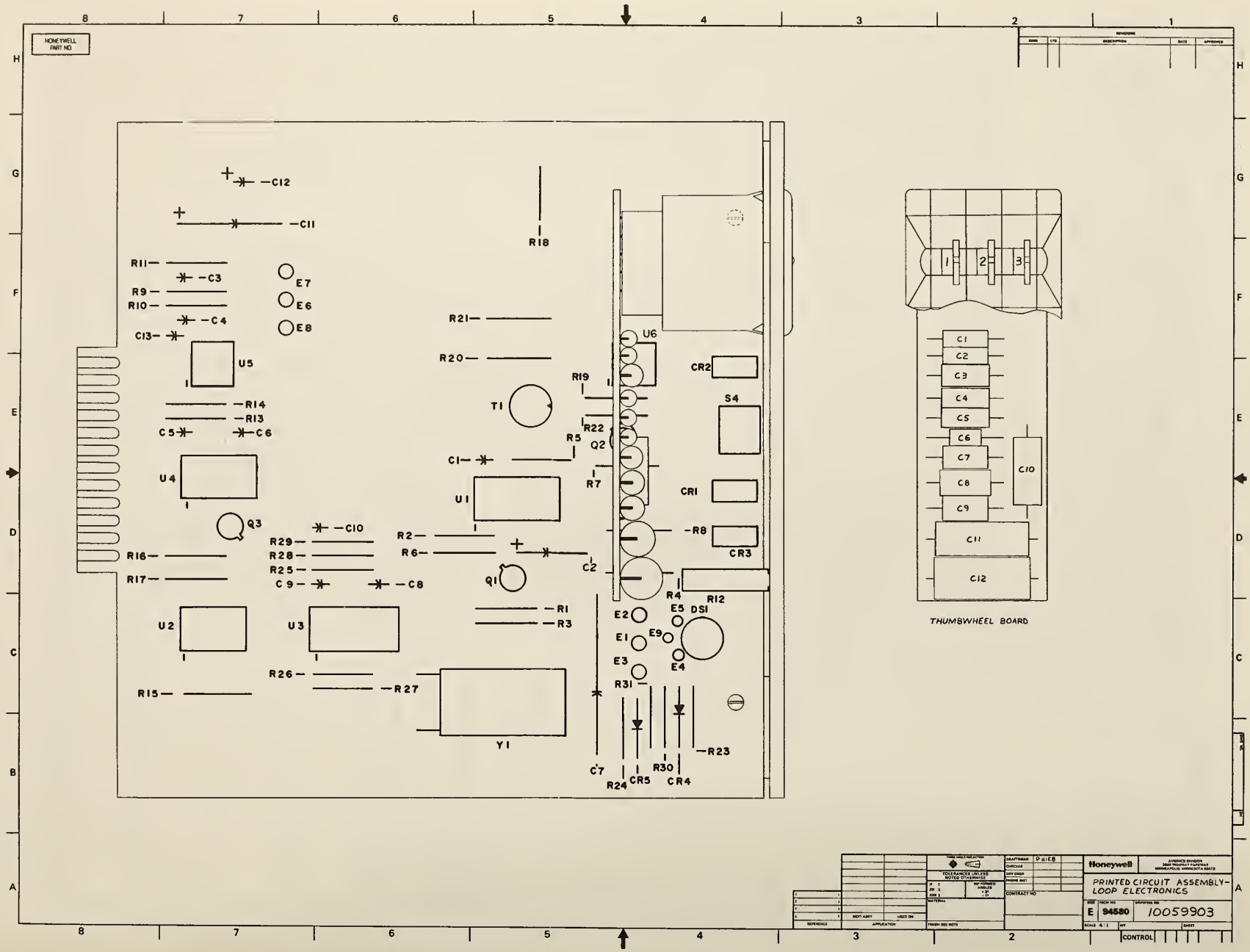
LOOP ELECTRONICS

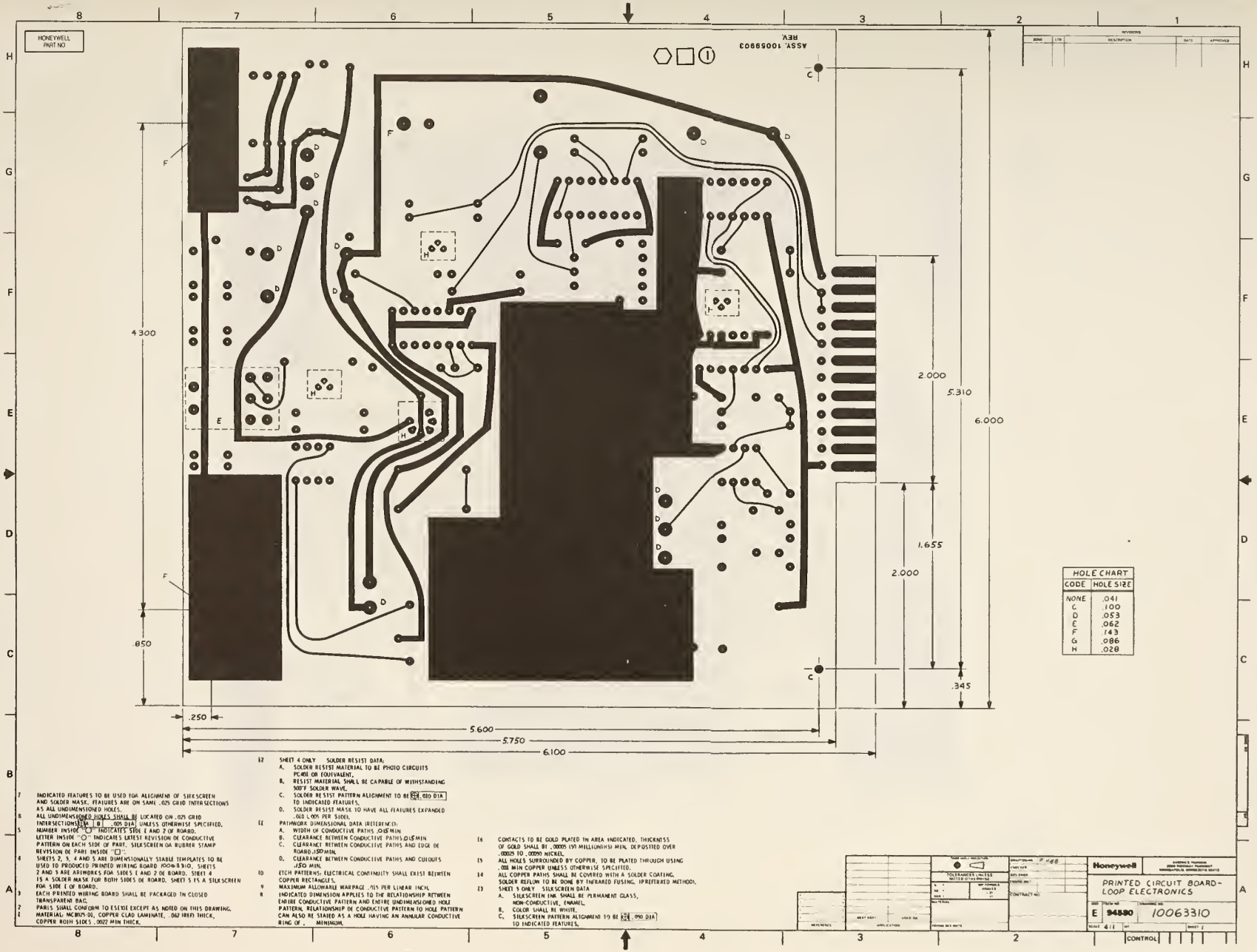
10059903

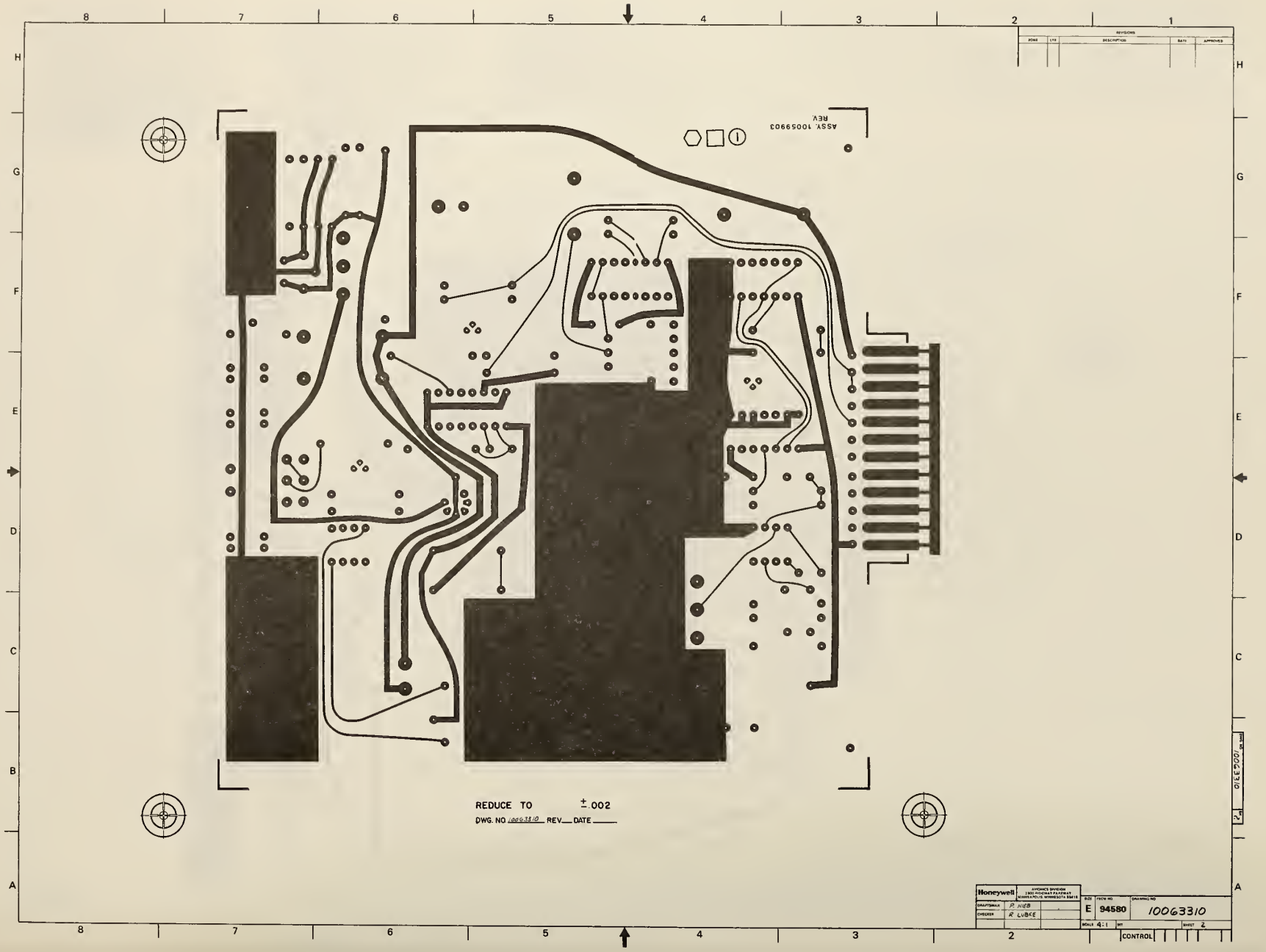
TYPED BY	PPRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				3	3

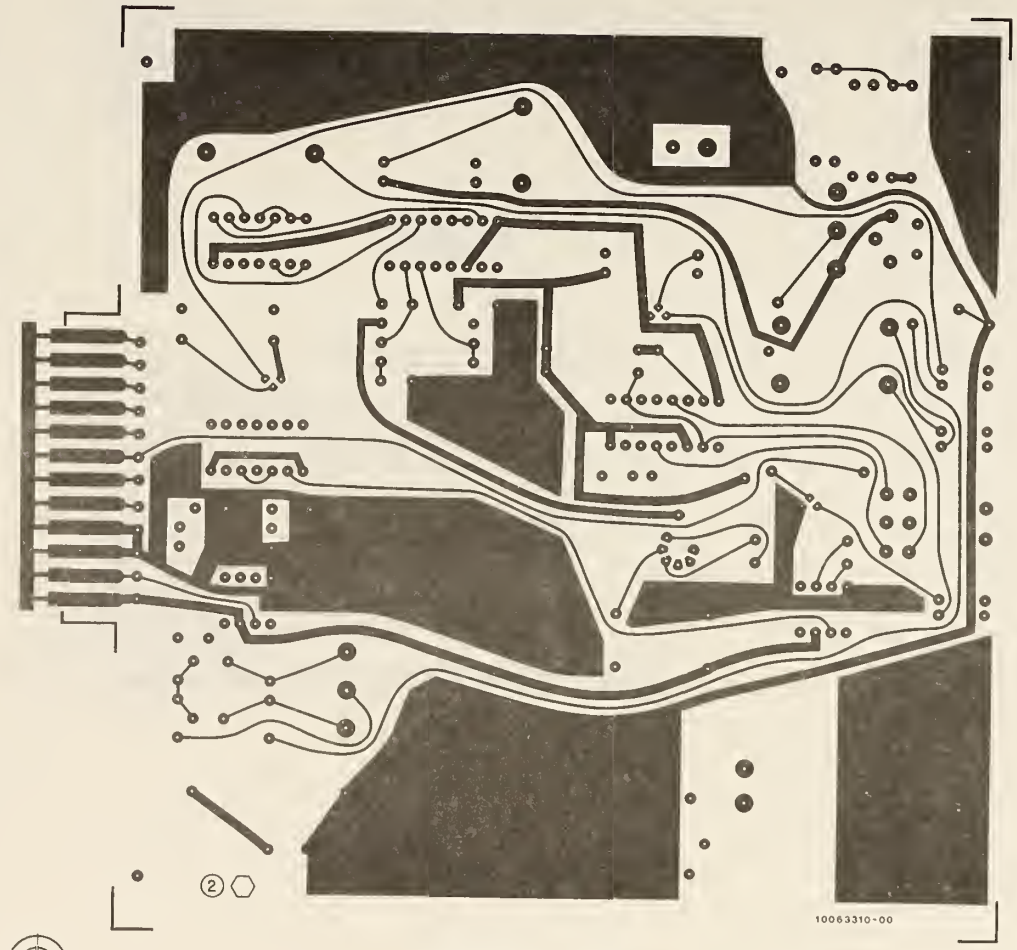
PART NO.	PART NAME							
SX482	CAPACITOR 82pF	1	C3	POLYSTYRENE-MALLORY				
SX316	CAPACITOR 160pF	1	C4					
SX320	CAPACITOR 200pF	1	C5					
SXM339	CAPACITOR 390pF	1	C6					
SXM382	CAPACITOR 820pF	1	C7					
SXM216	CAPACITOR 1600pF	1	C8					
SXM220	CAPACITOR .002	1	C9					
SXM239	CAPACITOR .0039	1	C10					
SXM282	CAPACITOR .0082	1	C11					
SXM116	CAPACITOR .016	1	C12					
SXM120	CAPACITOR .02	1	C7					
450-3704-01-03-00	PC JACK	6	J1,2				CAMBION	
461-2871-02-03-10	PLUG	2	P1,2				CAMBION	
RCR07G681JP	RESISTOR 680	2	R30,31					
CM04ED101J	CAPACITOR 100pF	1	C13					
10063324	PC BOARD-THUMBWHL	1						
10063310	PCBOARD	1						

HE-124


HONEYWELL PART NO.
C12
C11
R11
C3
R9
R10
C4
C13
E7
E6
E8
U5
R14
R13
C5
C6
U4
Q3
R16
R17
C10
R29
R28
R25
C9
C8
U2
U3
R26
R27
R15
Y1
R18
R21
R20
T1
R19
R22
R5
Q2
C1
U1
R7
R2
R6
Q1
C2
R1
R3
U6
CR2
S4
CR1
R8
CR3
R4
R12
E2
E5
DS1
E1
E9
E3
E4
R31
R23
C7
R24
CR5
R30
CR4
1
2
3
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
THUMBWHEEL BOARD
Honeywell
PRINTED CIRCUIT ASSEMBLY-
LOOP ELECTRONICS
E
94580
10059903
CONTROL


HONEYWELL PART NO
ASSY. 10068903
REV.
4.300
.850
.250
5.600
5.750
6.100
2.000
5.310
6.000
1.655
2.000
.345
HOLE CHART
CODE | HOLE SIZE
NONE | .041
C | .100
D | .053
E | .062
F | .143
G | .086
H | .028
7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.
6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS (A) (B) .005 DIA UNLESS OTHERWISE SPECIFIED.
5 NUMBER INSIDE "○" INDICATES SIDE E AND 2 OF BOARD. LETTER INSIDE "○" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".
4 SHEETS 2, 3, 4 AND 5 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCE PRINTED WIRING BOARD 10068310. SHEETS 2 AND 3 ARE ARTWORKS FOR SIDES E AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE E OF BOARD.
3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.
2 PARTS SHALL CONFORM TO ESCHE EXCEPT AS NOTED ON THIS DRAWING.
1 MATERIAL: MC8025-01, COPPER CLAD LAMINATE, .062 (REF) THICK, COPPER BOTH SIDES .0022 MIN THICK.
12 SHEET 4 ONLY SOLDER RESIST DATA:
A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC401 OR EQUIVALENT.
B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
C. SOLDER RESIST PATTERN ALIGNMENT TO BE (REF) .010 DIA TO INDICATED FEATURES.
D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 (.005 PER SIDE).
11 PATHWORK DIMENSIONAL DATA (REFERENCE):
A. WIDTH OF CONDUCTIVE PATHS .015 MIN
B. CLEARANCE BETWEEN CONDUCTIVE PATHS .015 MIN
C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD .150 MIN.
D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS .150 MIN.
10 ETCH PATTERNS; ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.
9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.
8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF . MINIMUM.
16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00005 (50 MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.
15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.
14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).
13 SHEET 5 ONLY SILKSCREEN DATA
A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
B. COLOR SHALL BE WHITE.
C. SILKSCREEN PATTERN ALIGNMENT TO BE (REF) .090 DIA TO INDICATED FEATURES.
TOLERANCES UNLESS NOTED OTHERWISE
Honeywell
PRINTED CIRCUIT BOARD-LOOP ELECTRONICS
E 94880 10063310
CONTROL


ASSY. 10059903
REV.
REDUCE TO ±.002
DWG. NO 10063310 REV. DATE
Honeywell
AVIONICS DIVISION
1300 HONEYWELL PARKWAY
MINNEAPOLIS, MINNESOTA 55416
DRAFTSMAN R. NIEB
CHECKER R. LUBKE
SIZE E
FSCM NO 94580
DRAWING NO 10063310
SCALE 4:1
WT
SHEET 2
CONTROL



REDUCE TO ±.002

DWG. NO. 10063310 REV.___ DATE _____

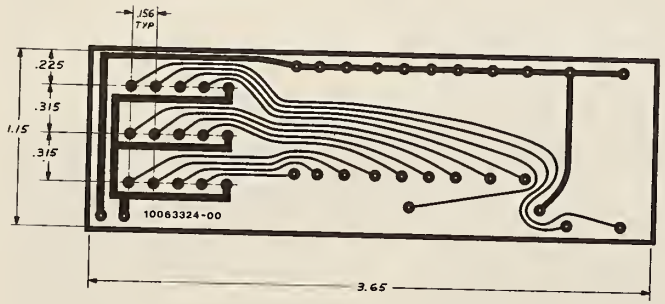
Honeywell

E 94580 10063310

CONTROL

HONEYWELL PART NO

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



HOLE CHART	
SYMBOL	HOLE SIZE
UNMARKED	.041

7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.

6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS [B | .005 DIA] UNLESS OTHERWISE SPECIFIED.

5 NUMBER INSIDE "○" INDICATES SIDE 1 AND 2 OF BOARD. LETTER INSIDE "○" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".

4 SHEETS 2, 3, 4 AND 5 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCED PRINTED WIRING BOARD 10063324. SHEETS 2 AND 3 ARE ARTWORKS FOR SIDES 1 AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE 1 OF BOARD.

3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.

2 PARTS SHALL CONFORM TO ES1301 EXCEPT AS NOTED ON THIS DRAWING.

1 MATERIAL: MC8025-01, COPPER CLAD LAMINATE, .062 (REF) THICK, COPPER BOTH SIDES, .0022 MIN THICK.

12 SHEET 4 ONLY SOLDER RESIST DATA:
- A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC401 OR EQUIVALENT.
- B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
- C. SOLDER RESIST PATTERN ALIGNMENT TO BE [⊕ .010 DIA] TO INDICATED FEATURES.
- D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .020 (.005 PER SIDE).

11 PATHWORK DIMENSIONAL DATA (REFERENCE):
- A. WIDTH OF CONDUCTIVE PATHS .015 MIN
- B. CLEARANCE BETWEEN CONDUCTIVE PATHS .015 MIN
- C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD .150 MIN.
- D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS .150 MIN.

10 ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.

9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.

8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATERNAL RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF , MINIMUM.

16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00005 (5) MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.

15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.

14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).

13 SHEET 5 ONLY SILKSCREEN DATA:
- A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
- B. COLOR SHALL BE WHITE.
- C. SILKSCREEN PATTERN ALIGNMENT TO BE [⊕ .050 DIA] TO INDICATED FEATURES.

REFERENCE	NEXT ASSY	USED ON

APPLICATION

THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED OTHERWISE: X ± .XX ± .XXX ± BEND ANGLES ± °

MATERIAL

FINISH SEE NOTE

DRAFTSMAN	H. JOHNSON
CHECKER	
DEV ENGR	
ENGRG MGT	
CONTRACT NO	

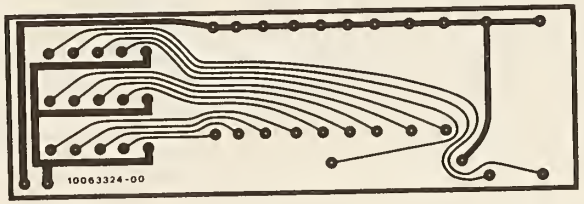
Honeywell — AVIONICS DIVISION, 2600 ROCKWY PARKWAY, MINNEAPOLIS, MINNESOTA 55413

PRINTED CIRCUIT BOARD — THUMBWHEEL

SIZE E | FSCM NO 94580 | DRAWING NO 10063324

SCALE 0:1 | WT | SHEET 2

CONTROL



REDUCE TO ±.002

DWG. NO 10063324 REV. ___ DATE ___

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

Honeywell

SYSTEMS DIVISION
2600 RIDGEWAY PARKWAY
MINNEAPOLIS, MINNESOTA 55413

DRAWN R. ZIB
CHECKED A. LUBKE

SIZE E | FSCM NO 94580 | DRAWING NO 10063324

SCALE 2:1 | WT | SHEET 2

CONTROL

10063324 R2

Honeywell

PRINTED IN U. S. A.

SUPERSEDES
SUPERSEDED BY

ENGINEERING PARTS LIST

REV.	DATE	E.O.	REV.	DATE	E.O.
A	7-12-77				
B	7-29-77				
C	10-6-77				
D	10-10-77				

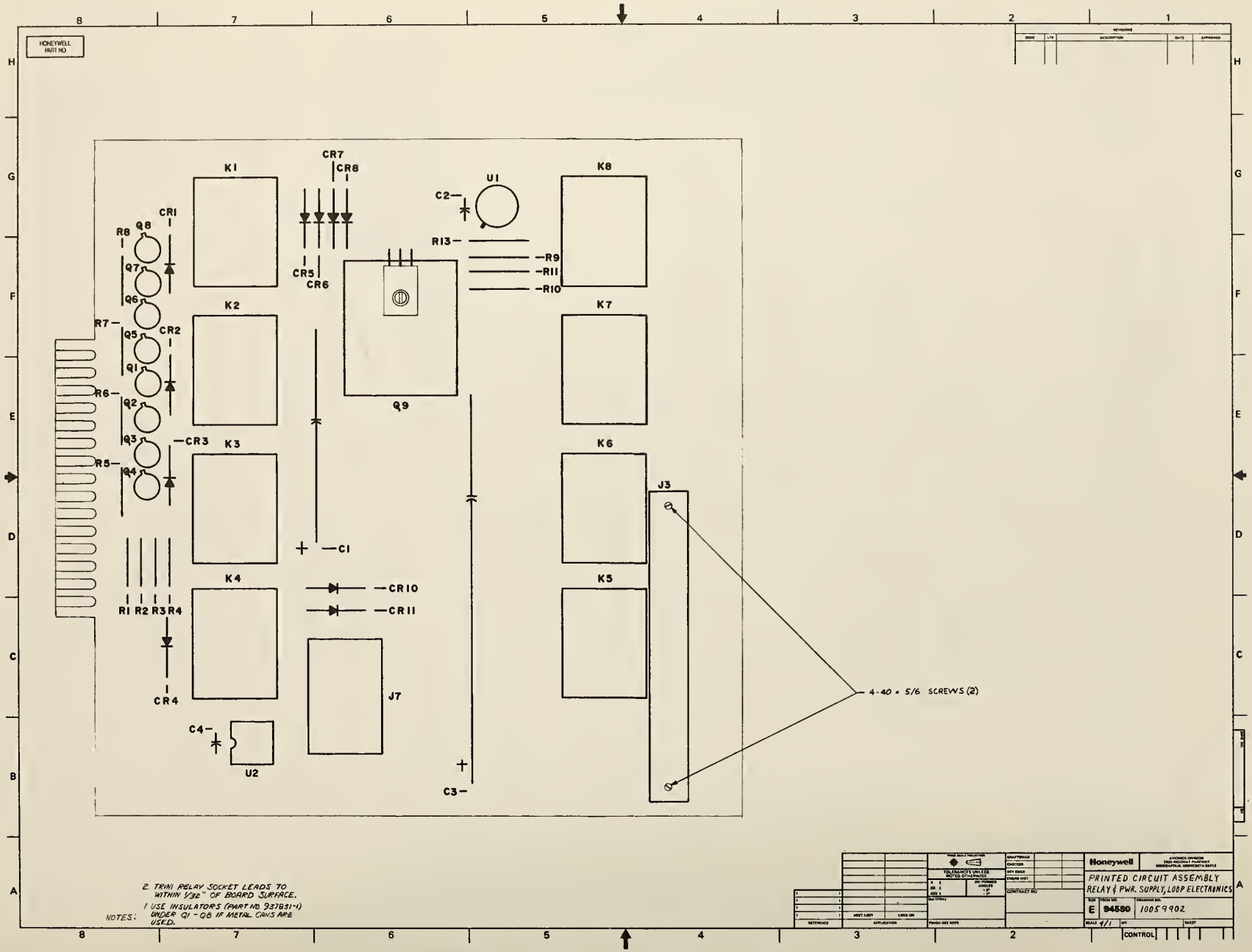
POWER SUPPLY
LOOP ELECTRONICS

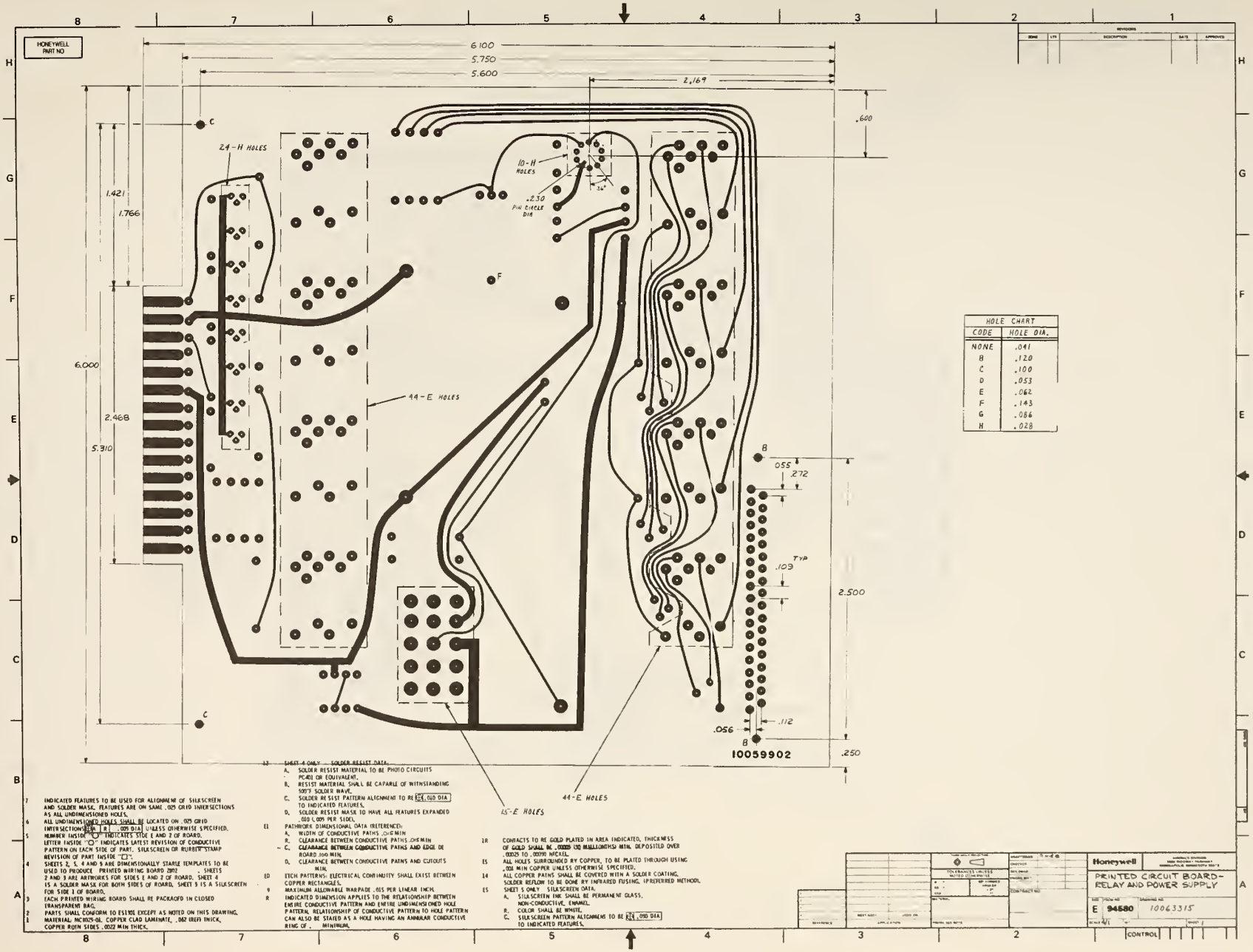
10059902

TYPED BY	PRRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.
				1	1

PART NO.	PART NAME	QTY							
CA3130	OP AMPL	1	U2						
723L	VOLTAGE REG	1	U1						
2N2222	TRANSISTOR	8	Q1	THRU	Q8				
2N5298	TRANSISTOR	1	Q9						
1N4384	RECTIFIER	2	CR10,	11					
1N4454	DIODE	8	CR1	THRU	CR8				
RCR07G391J	RESISTOR 390	1	R13						
RCR07G103J	RESISTOR 10K	8	R1	THRU	R8				
RCR20G1R0J	RESISTOR 1	1	R11						
RN55D6801F	RESISTOR 681	1	R9						
RN55D1001F	RESISTOR 1K	1	R10						
CM04ED101J	CAPACITOR 100pF	1	C2,	C4					
501U025DIN	CAPACITOR 500	1	C1						
232U050N3C	CAPACITOR 2300	1	C3						
AZ420-V50-4H	RELAY	8	K1	THRU	K8	AMERICAN-ZEITLER			
ST140-A1	RELAY SOCKET	8				AMERICAN-ZEITLER			
ST140-1	RETAINER	8				AMERICAN-ZEITLER			
205859-2	CONNECTOR, RTANG	1	J3						
03-09-2153	PLUG	1	J7					MOLEX	
02-09-2134	CONTACT, MALE	12							
6-32 UNC x .38 LG	SCREW, PAN HEAD	2							
NO. 6	LOCKWASHER	2							
6-32	NUT, HEX	2							
10063315	PC BOARD	1							

HE-124

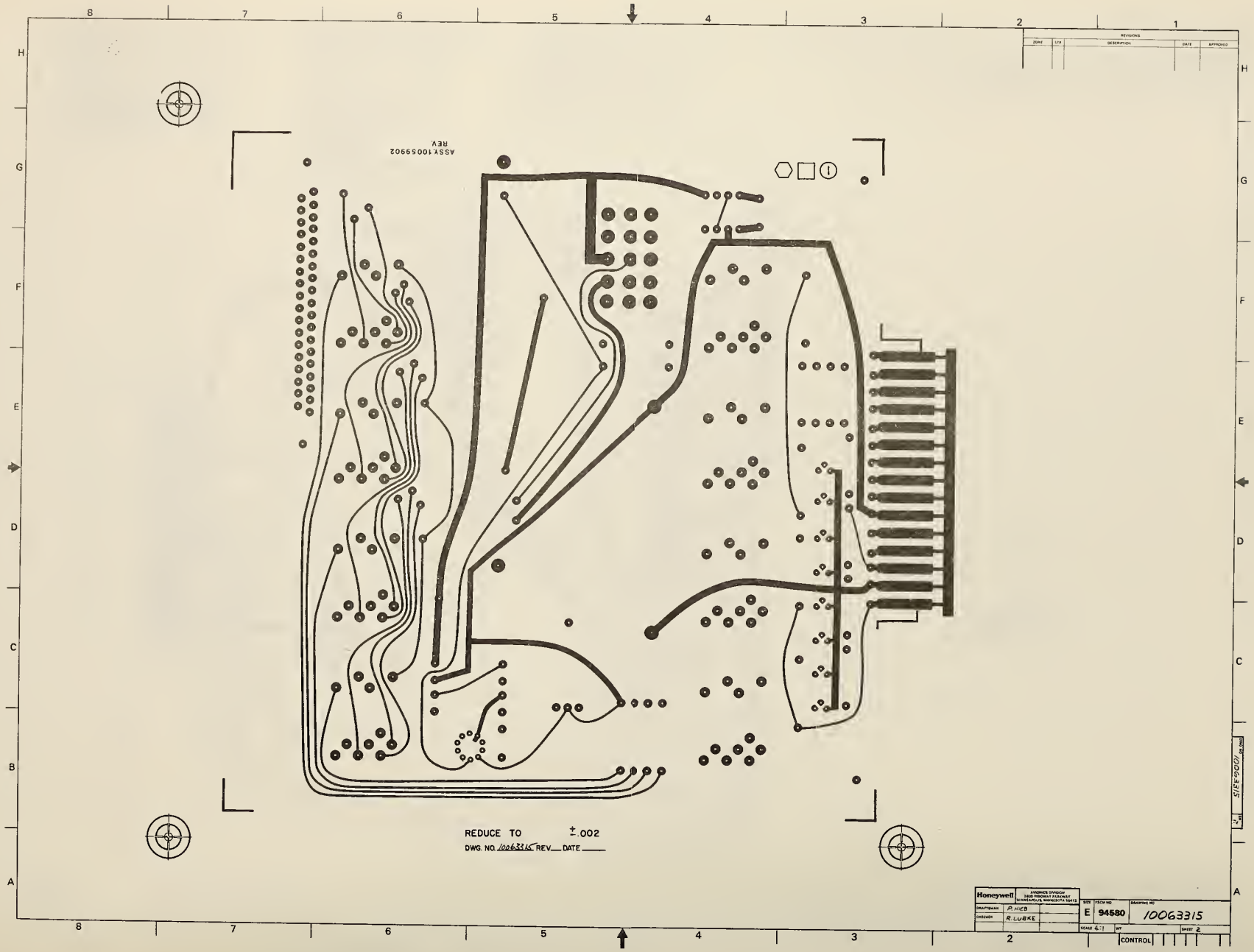

HONEYWELL PART NO.
K1
K2
K3
K4
K5
K6
K7
K8
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR10
CR11
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R13
U1
U2
C1
C2
C3
C4
J3
J7
4-40 x 5/16 SCREWS (2)
NOTES:
2. TRIM RELAY SOCKET LEADS TO WITHIN 1/32" OF BOARD SURFACE.
1 USE INSULATORS (PART NO. 937B31-1) UNDER Q1 - Q8 IF METAL CANS ARE USED.
Honeywell
PRINTED CIRCUIT ASSEMBLY
RELAY & PWR. SUPPLY, LOOP ELECTRONICS
E
94580
1005 9902
CONTROL

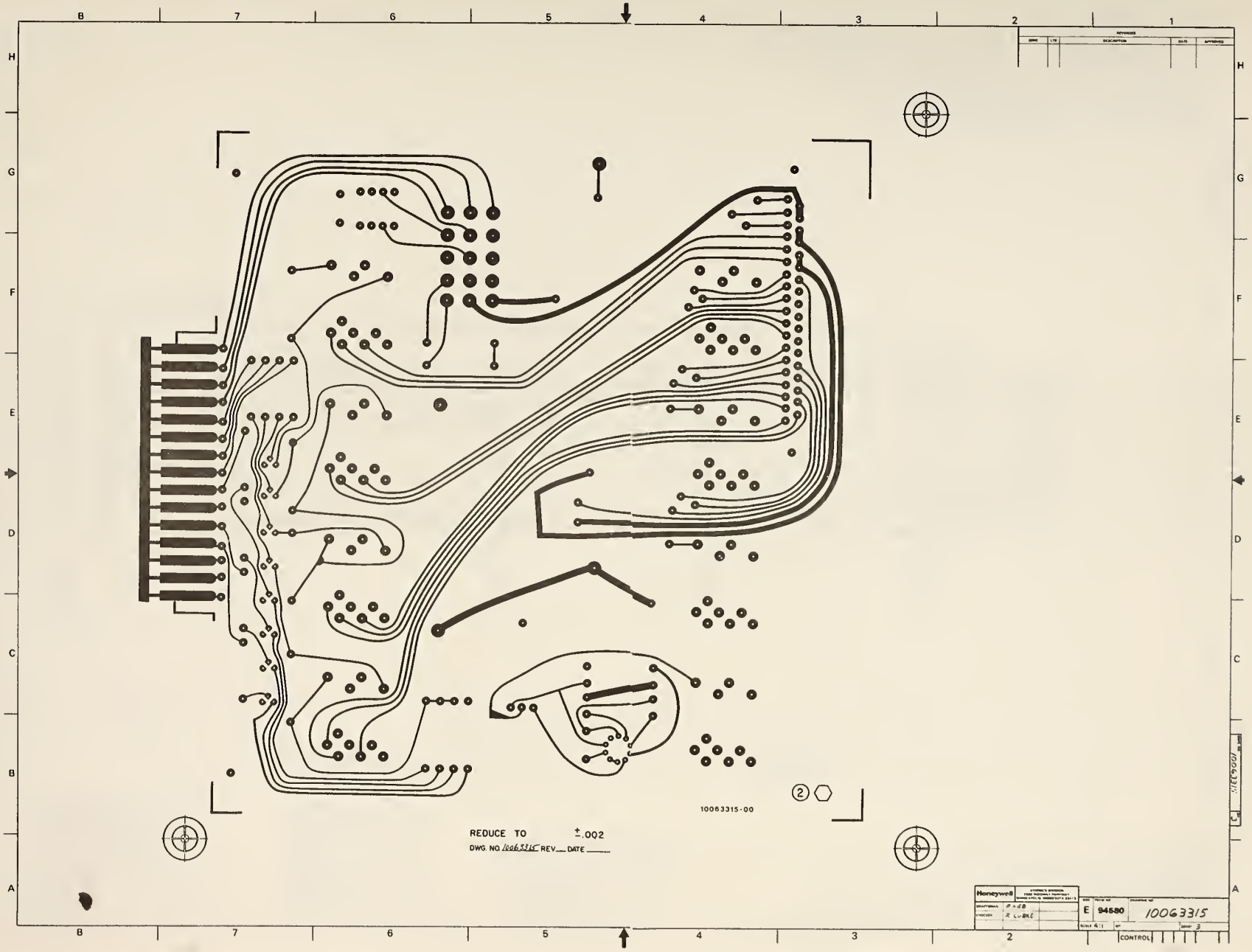


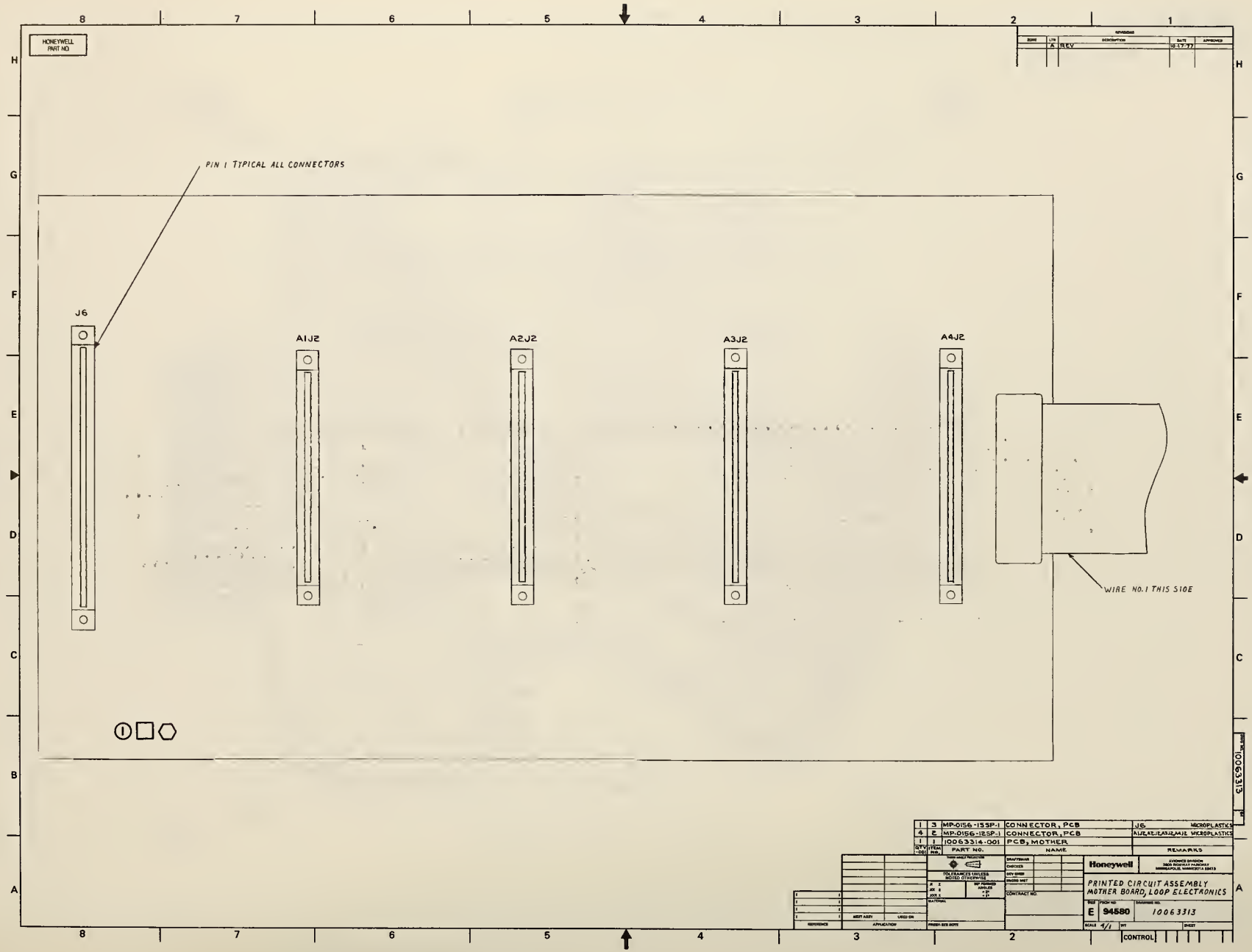
7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.
6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS [illegible] .005 DIA UNLESS OTHERWISE SPECIFIED.
5 NUMBER INSIDE "O" INDICATES SIDE E AND 2 OF BOARD. LETTER INSIDE "O" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".
4 SHEETS 2, 5, 4 AND 9 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCE PRINTED WIRING BOARD 2092 , SHEETS 2 AND 3 ARE ARTWORKS FOR SIDES E AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE 2 OF BOARD.
3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.
2 PARTS SHALL CONFORM TO ESTMS EXCEPT AS NOTED ON THIS DRAWING.
1 MATERIAL MC1025-01. COPPER CLAD LAMINATE, .062 (REF) THICK, COPPER BOTH SIDES .0022 MIN THICK.

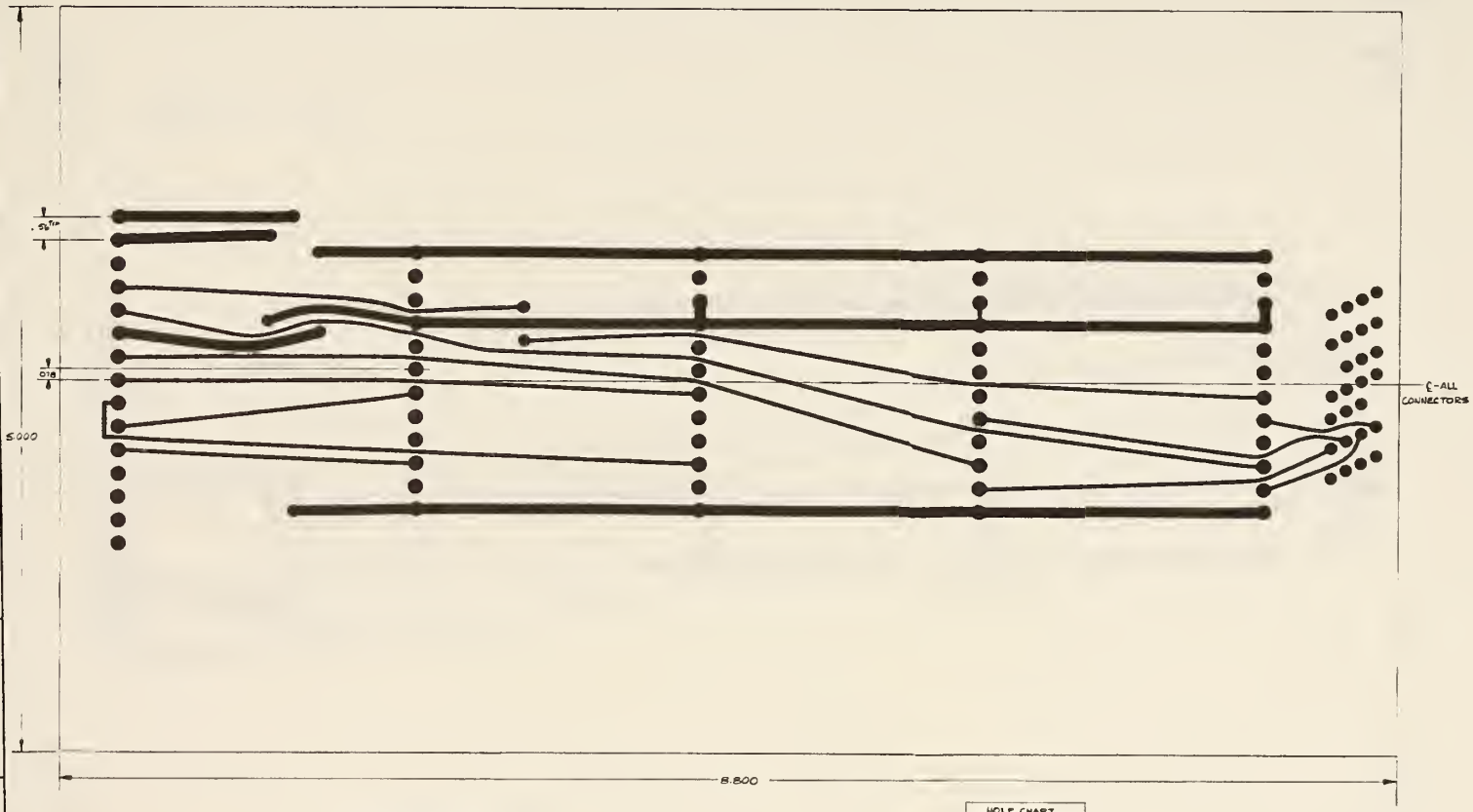
13 SHEET 4 ONLY SOLDER RESIST DATA.
A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC401 OR EQUIVALENT.
B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
C. SOLDER RESIST PATTERN ALIGNMENT TO BE [illegible] .010 DIA TO INDICATED FEATURES.
D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 (.005 PER SIDE).
E1 PATHWORK DIMENSIONAL DATA (REFERENCE):
A. WIDTH OF CONDUCTIVE PATHS .010 MIN
B. CLEARANCE BETWEEN CONDUCTIVE PATHS .010 MIN
C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD .100 MIN.
D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS MIN.
ED ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.
9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.
R INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF . MINIMUM.

1R CONTACTS TO BE GOLD PLATED IN AREA INDICATED, THICKNESS OF GOLD SHALL BE .00005 (50 MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.
E5 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.
14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).
E5 SHEET 5 ONLY SILKSCREEN DATA.
A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
B. COLOR SHALL BE WHITE.
C. SILKSCREEN PATTERN ALIGNMENT TO BE [illegible] .010 DIA TO INDICATED FEATURES.


ASSY 100 59902
REV
REDUCE TO ±.002
DWG. NO. 10063315 REV. DATE
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
Honeywell
AVIONICS DIVISION
1600 TRUNKAY PARKWAY
MINNEAPOLIS, MINNESOTA 55413
DRAFTSMAN P. WEB
CHECKER R. LUBKE
SIZE E
FSCM NO 94580
DRAWING NO 10063315
SCALE 4:1
WT
SHEET 2
CONTROL
SIZE-9001


REVISIONS
SYMB
LTR
DESCRIPTION
DATE
APPROVED
10063315-00
REDUCE TO ±.002
DWG. NO. 10063315 REV. DATE
Honeywell
SYSTEMS DIVISION
1900 RUDOLPH, MINNEAPOLIS, MINNESOTA 55413
DRAFTSMAN R.H.B.
CHECKED R. LUBKE
SIZE E
94580
DRAWING NO 10063315
SCALE 4:1
SHEET 3
CONTROL
SHEET 10063315


HONEYWELL PART NO.
REVISIONS
REV
PIN 1 TYPICAL ALL CONNECTORS
J6
A1J2
A2J2
A3J2
A4J2
WIRE NO. 1 THIS SIDE
1 3 MP-0156-155P-1 CONNECTOR, PCB J6 MICROPLASTICS
4 2 MP-0156-125P-1 CONNECTOR, PCB A1J2, A2J2, A3J2, A4J2 MICROPLASTICS
1 1 10063314-001 PCB, MOTHER
QTY REQ. ITEM NO. PART NO. NAME REMARKS
Honeywell
AVIONICS DIVISION
3660 RIDGEWAY PARKWAY
MINNEAPOLIS, MINNESOTA 55413
PRINTED CIRCUIT ASSEMBLY
MOTHER BOARD, LOOP ELECTRONICS
E 94580
10063313
SCALE 4/1
CONTROL
10063313



HONEYWELL PART NO

HOLE CHART	
SYMBOL	HOLE SIZE
UNMARKED	.041

7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.

6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS. [illegible] .005 DIA UNLESS OTHERWISE SPECIFIED.

5 NUMBER INSIDE "O" INDICATES SIDE 1 AND 2 OF BOARD. LETTER INSIDE "O" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".

4 SHEETS 2, 3, 4 AND 5 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCE PRINTED WIRING BOARD [illegible]. SHEETS 2 AND 5 ARE ARTWORKS FOR SIDES 1 AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE 1 OF BOARD.

3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.

2 PARTS SHALL CONFORM TO ES1301 EXCEPT AS NOTED ON THIS DRAWING.

1 MATERIAL MC8025-01, COPPER CLAD LAMINATE, .062 (REF) THICK, COPPER BOTH SIDES, .0027 MIN THICK.

12 SHEET 4 ONLY SOLDER RESIST DATA:
- A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC401 OR EQUIVALENT.
- B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
- C. SOLDER RESIST PATTERN ALIGNMENT TO BE [illegible] .010 DIA TO INDICATED FEATURES.
- D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 (.005 PER SIDE).

11 PATHFORM DIMENSIONAL DATA (REFERENCE):
- A. WIDTH OF CONDUCTIVE PATHS [illegible] MIN
- B. CLEARANCE BETWEEN CONDUCTIVE PATHS [illegible] MIN
- C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD [illegible] MIN.
- D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS [illegible] MIN.

10 ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.

9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.

8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF [illegible] MINIMUM.

16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00005 (50 MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.

15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.

14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING, IF PREFERRED METHOD.

15 SHEET 5 ONLY SILKSCREEN DATA.
- A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
- B. COLOR SHALL BE WHITE.
- C. SILKSCREEN PATTERN ALIGNMENT TO BE [illegible] .050 DIA TO INDICATED FEATURES.

TOLERANCES UNLESS NOTED OTHERWISE

NEXT ASSY | USED ON | APPLICATION

CONTRACT NO

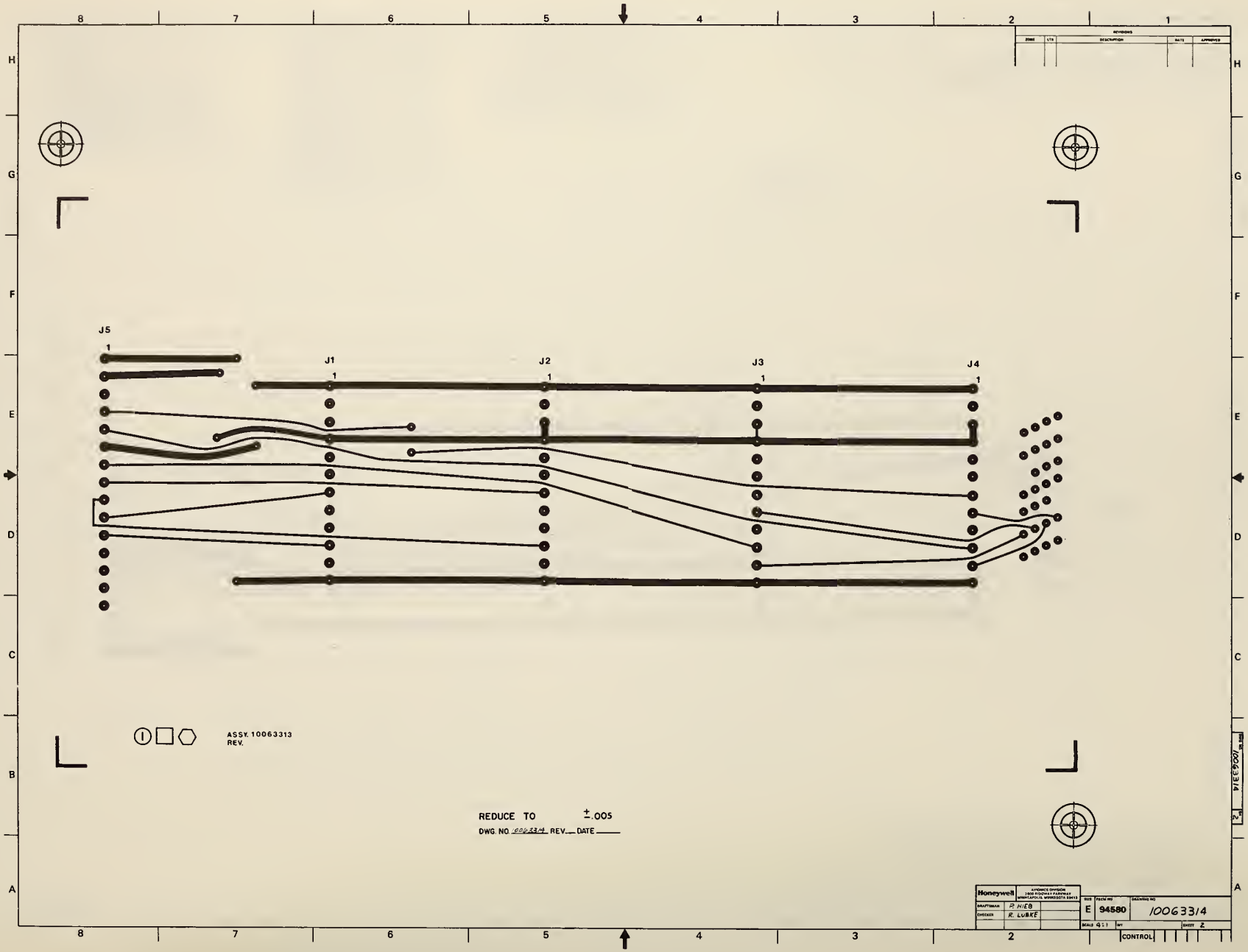
Honeywell

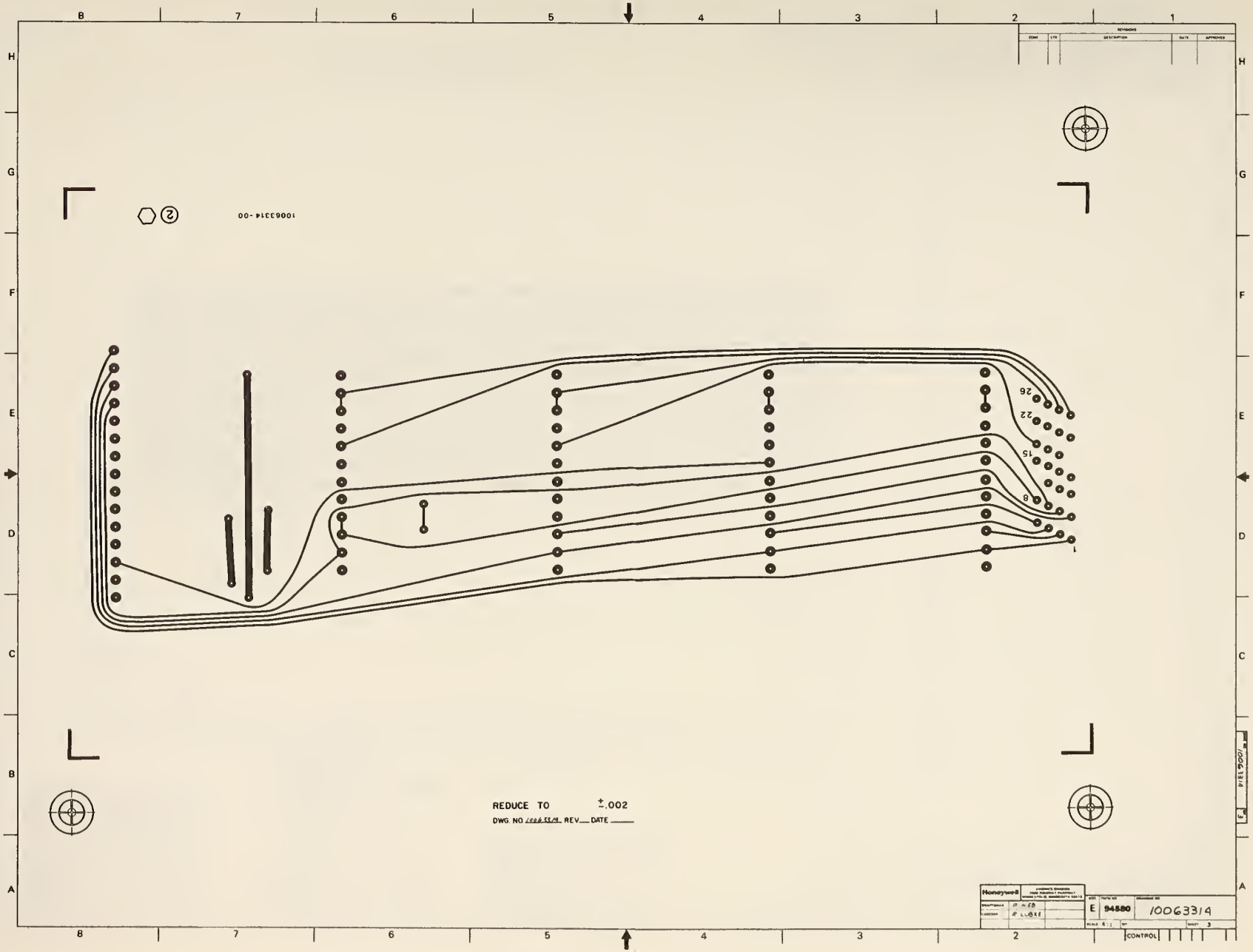
PRINTED CIRCUIT BOARD—LOOP ELECTRONICS MOTHER BOARD

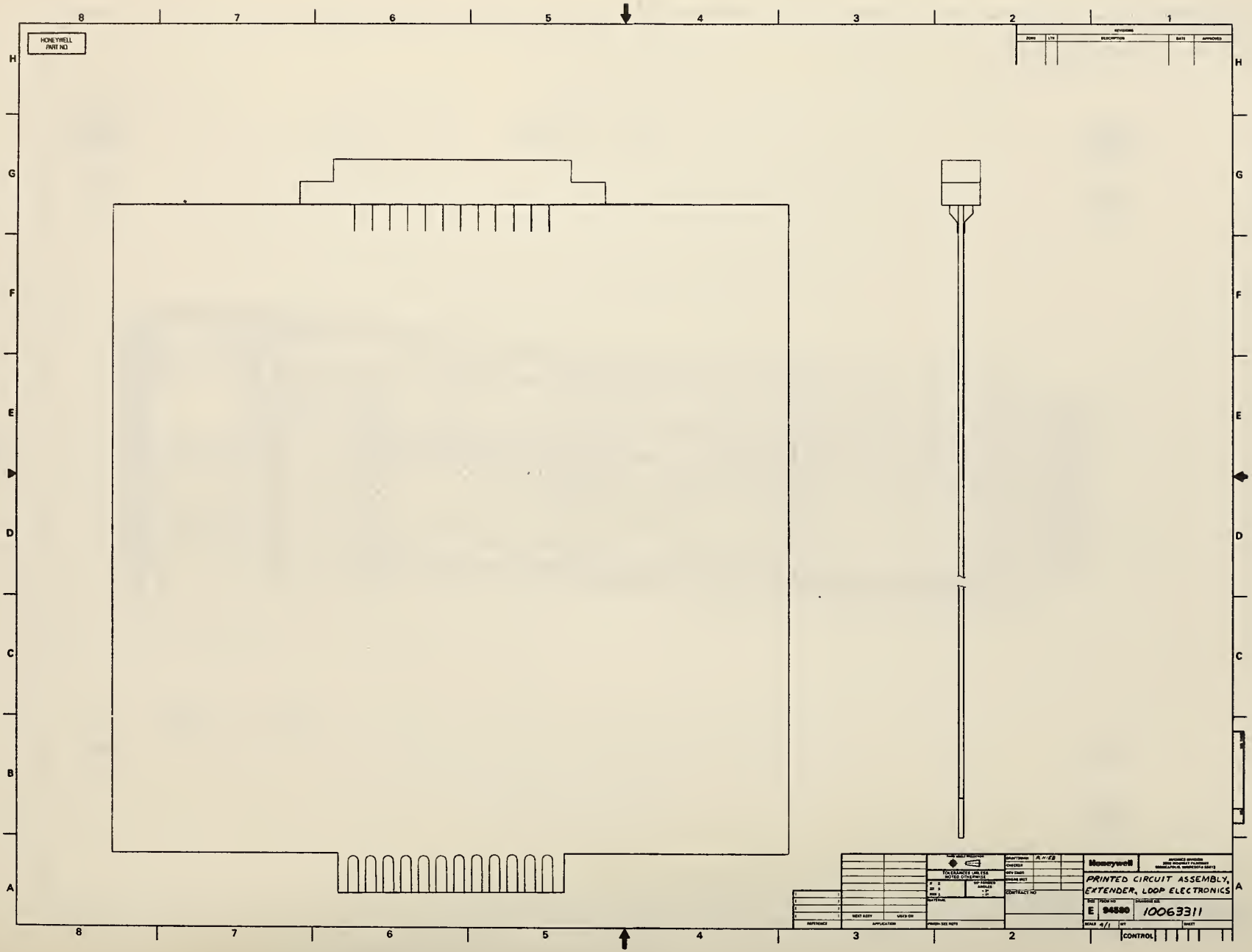
SIZE E | CODE IDENT NO 94880 | DRAWING NO 10163514

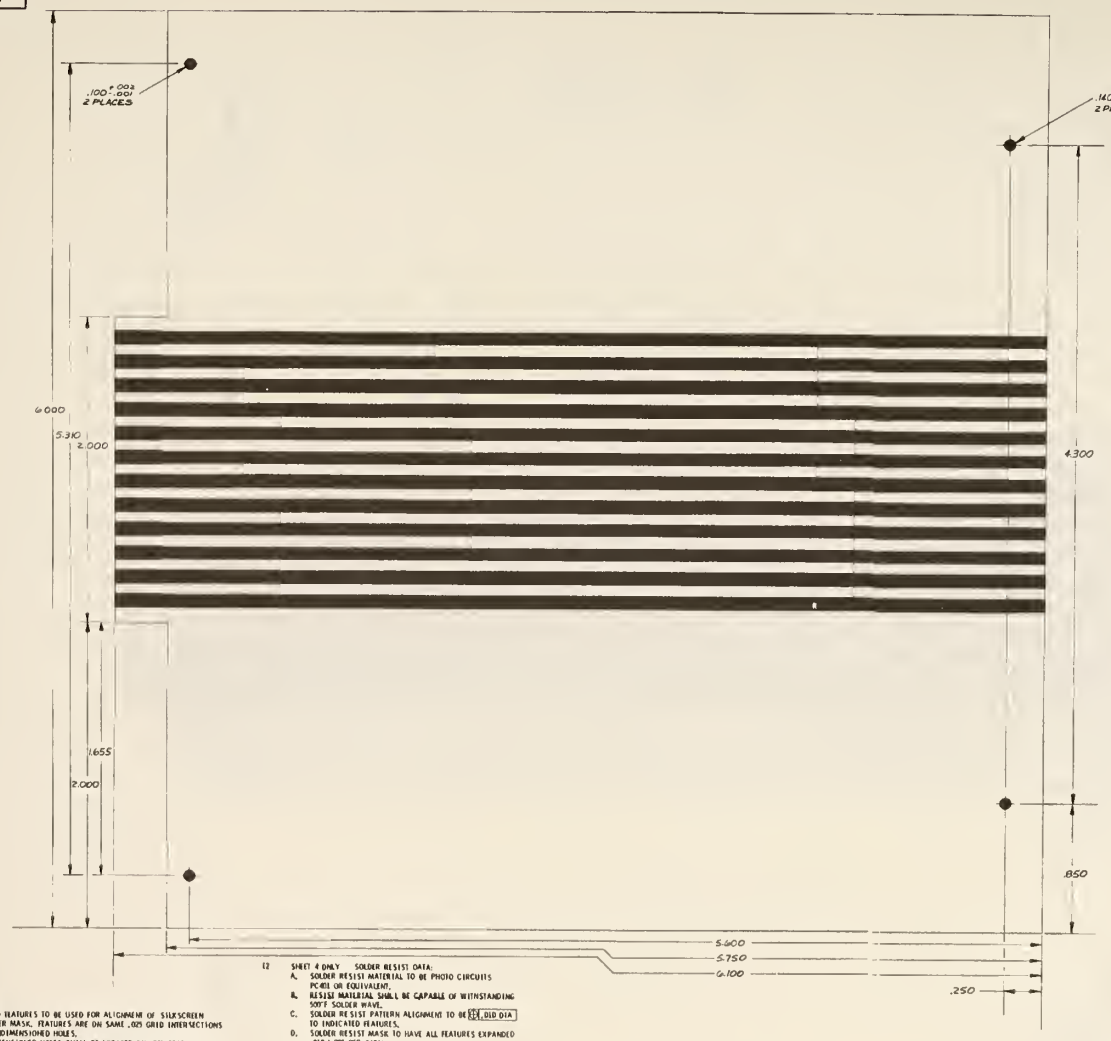
SCALE 6:1 | SHEET 1

CONTROL


J5
1
J1
1
J2
1
J3
1
J4
1
ASSY. 10063313
REV.
REDUCE TO ±.005
DWG. NO. 10063314 REV. DATE
Honeywell
AVIONICS DIVISION
1600 FIDDLER'S PARKWAY
MINNEAPOLIS, MINNESOTA 55413
DRAFTSMAN R. HEB
CHECKER R. LUKKE
SIZE E
FSCM NO 94580
DRAWING NO 10063314
SCALE 4:1
SHEET 2
CONTROL


REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
10063314-00
26
22
15
8
1
REDUCE TO ±.002
DWG. NO 10063314 REV. DATE
Honeywell
E
94580
10063314
SCALE 4:1
SHEET 3
CONTROL


HONEYWELL PART NO
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
DRAFTSMAN
R.H.E.B.
CHECKER
APPV ENGR
APPV EMGR
DRAWING SHUT
CONTRACT NO
TOLERANCE UNLESS NOTED OTHERWISE
MATERIAL
NEXT ASSY
USED ON
REFERENCE
APPLICATION
Honeywell
PRINTED CIRCUIT ASSEMBLY, EXTENDER, LOOP ELECTRONICS
SIZE
E
FSCM NO
94580
DRAWING NO
10063311
SCALE 4/1
WT
SHEET
CONTROL



7 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SILKSCREEN AND SOLDER MASK. FEATURES ARE ON SAME .025 GRID INTERSECTIONS AS ALL UNDIMENSIONED HOLES.

6 ALL UNDIMENSIONED HOLES SHALL BE LOCATED ON .025 GRID INTERSECTIONS [B] [B] .025 DIA UNLESS OTHERWISE SPECIFIED.

5 NUMBER INSIDE "⬡" INDICATES SIDE 1 AND 2 OF BOARD. LETTER INSIDE "⬡" INDICATES LATEST REVISION OF CONDUCTIVE PATTERN ON EACH SIDE OF PART. SILKSCREEN OR RUBBER STAMP REVISION OF PART INSIDE "□".

4 SHEETS 2, 3, 4 AND 5 ARE DIMENSIONALLY STABLE TEMPLATES TO BE USED TO PRODUCE PRINTED WIRING BOARD [illegible]. SHEETS 2 AND 3 ARE ARTWORKS FOR SIDES 1 AND 2 OF BOARD. SHEET 4 IS A SOLDER MASK FOR BOTH SIDES OF BOARD. SHEET 5 IS A SILKSCREEN FOR SIDE 1 OF BOARD.

3 EACH PRINTED WIRING BOARD SHALL BE PACKAGED IN CLOSED TRANSPARENT BAG.

2 PARTS SHALL CONFORM TO ESS9B EXCEPT AS NOTED ON THIS DRAWING.

1 MATERIAL MC8025-01, COPPER CLAD LAMINATE, .062 (REF) THICK, COPPER BOTH SIDES .0022 MIN THICK.

12 SHEET 4 ONLY SOLDER RESIST DATA:
- A. SOLDER RESIST MATERIAL TO BE PHOTO CIRCUITS PC401 OR EQUIVALENT.
- B. RESIST MATERIAL SHALL BE CAPABLE OF WITHSTANDING 500°F SOLDER WAVE.
- C. SOLDER RESIST PATTERN ALIGNMENT TO BE [C] .010 DIA TO INDICATED FEATURES.
- D. SOLDER RESIST MASK TO HAVE ALL FEATURES EXPANDED .010 ±.005 PER SIDE.

11 PATTERNS DIMENSIONAL DATA (REFERENCE):
- A. WIDTH OF CONDUCTIVE PATHS .025 MIN
- B. CLEARANCE BETWEEN CONDUCTIVE PATHS .025 MIN
- C. CLEARANCE BETWEEN CONDUCTIVE PATHS AND EDGE OF BOARD .100 MIN.
- D. CLEARANCE BETWEEN CONDUCTIVE PATHS AND CUTOUTS .100 MIN.

10 ETCH PATTERNS: ELECTRICAL CONTINUITY SHALL EXIST BETWEEN COPPER RECTANGLES.

9 MAXIMUM ALLOWABLE WARPAGE .015 PER LINEAR INCH.

8 INDICATED DIMENSION APPLIES TO THE RELATIONSHIP BETWEEN ENTIRE CONDUCTIVE PATTERN AND ENTIRE UNDIMENSIONED HOLE PATTERN. RELATIONSHIP OF CONDUCTIVE PATTERN TO HOLE PATTERN CAN ALSO BE STATED AS A HOLE HAVING AN ANNULAR CONDUCTIVE RING OF , MINIMUM.

16 CONTACTS TO BE GOLD PLATED IN AREA INDICATED. THICKNESS OF GOLD SHALL BE .00005 (50 MILLIONTHS) MIN. DEPOSITED OVER .00025 TO .00050 NICKEL.

15 ALL HOLES SURROUNDED BY COPPER, TO BE PLATED THROUGH USING .001 MIN COPPER UNLESS OTHERWISE SPECIFIED.

14 ALL COPPER PATHS SHALL BE COVERED WITH A SOLDER COATING. SOLDER REFLOW TO BE DONE BY INFRARED FUSING. (PREFERRED METHOD).

13 SHEET 5 ONLY SILKSCREEN DATA:
- A. SILKSCREEN INK SHALL BE PERMANENT GLASS, NON-CONDUCTIVE, ENAMEL.
- B. COLOR SHALL BE WHITE.
- C. SILKSCREEN PATTERN ALIGNMENT TO BE [C] .010 DIA TO INDICATED FEATURES.

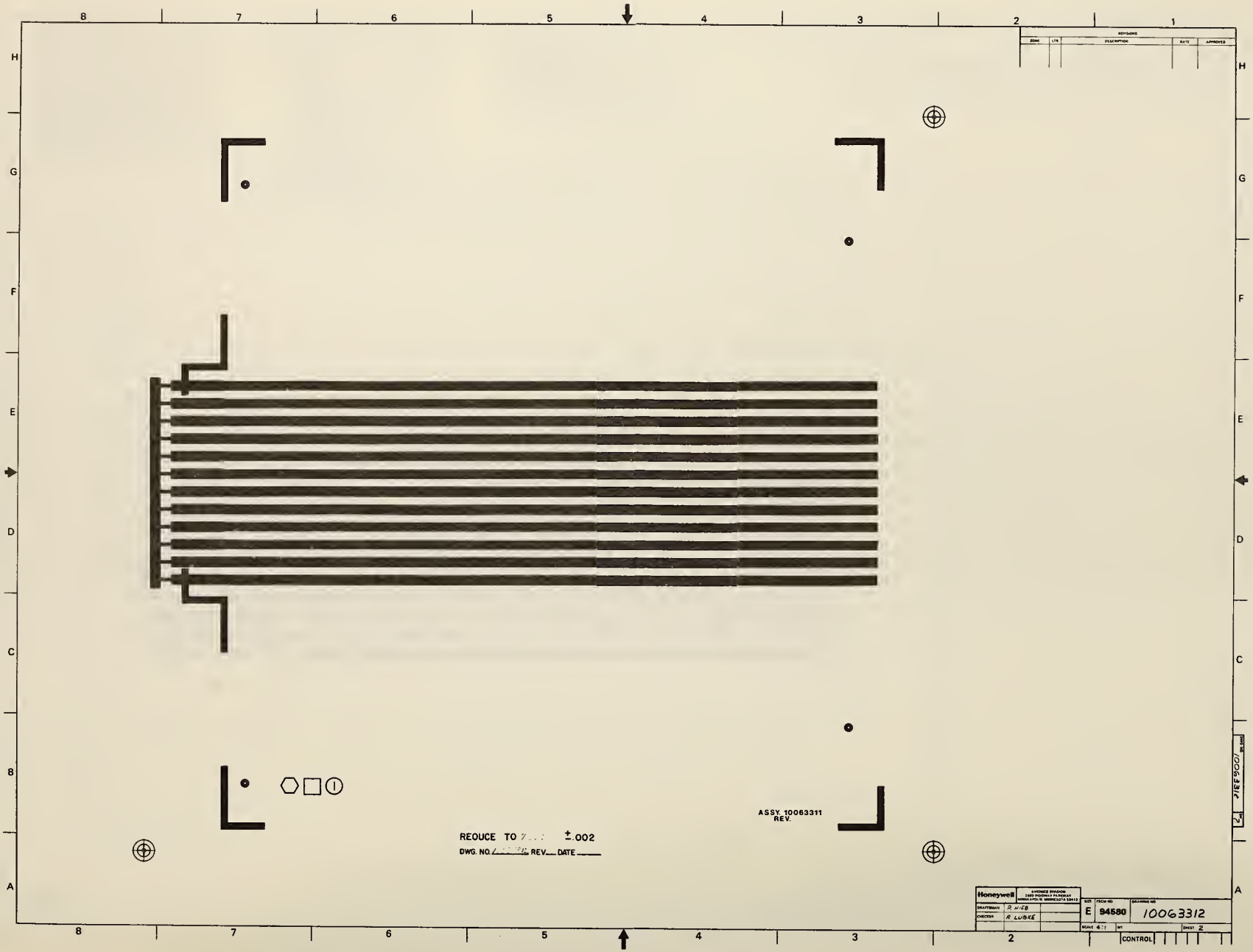
ZONE	LTR	DESCRIPTION	DATE	APPROVED

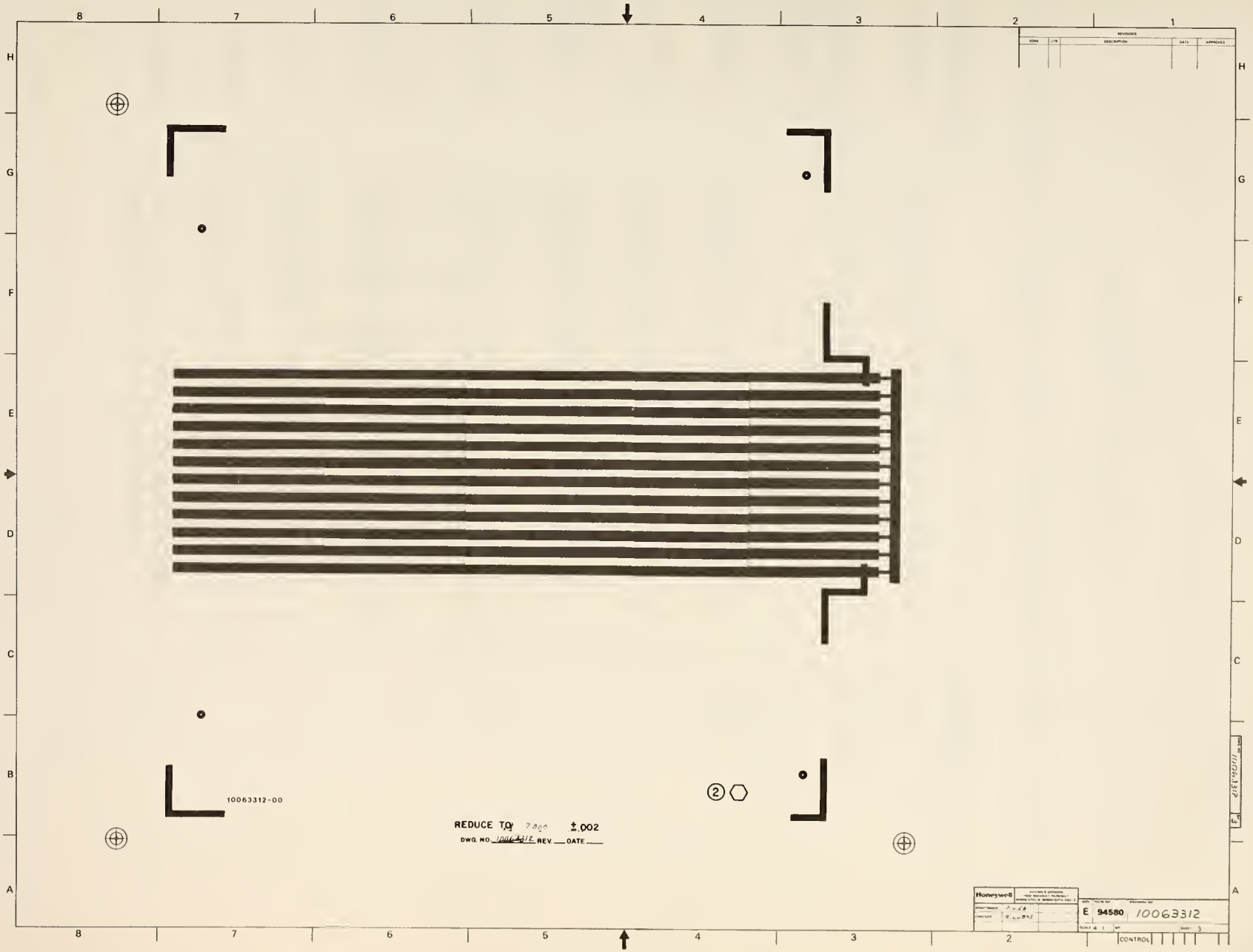
Honeywell

PRINTED CIRCUIT BOARD-EXTENDER

E 94580 100653312

CONTROL


REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
REDUCE TO 7 : 1 ±.002
DWG. NO. 7 REV. DATE
ASSY 10063311
REV.
Honeywell
DRAFTSMAN R HIEB
CHECKER R LUSKE
SIZE E
FSCM NO 94580
DRAWING NO 10063312
SCALE 4:1
SHEET 2
CONTROL
10063311 REV 7


REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
10063312-00
REDUCE TO 7000 ±.002
DWG. NO. 10063312 REV. DATE
Honeywell
E 94580 10063312
CONTROL

SECTION 7
SCHEMATIC DIAGRAMS

The following schematic diagrams/signal list are presented in this section:

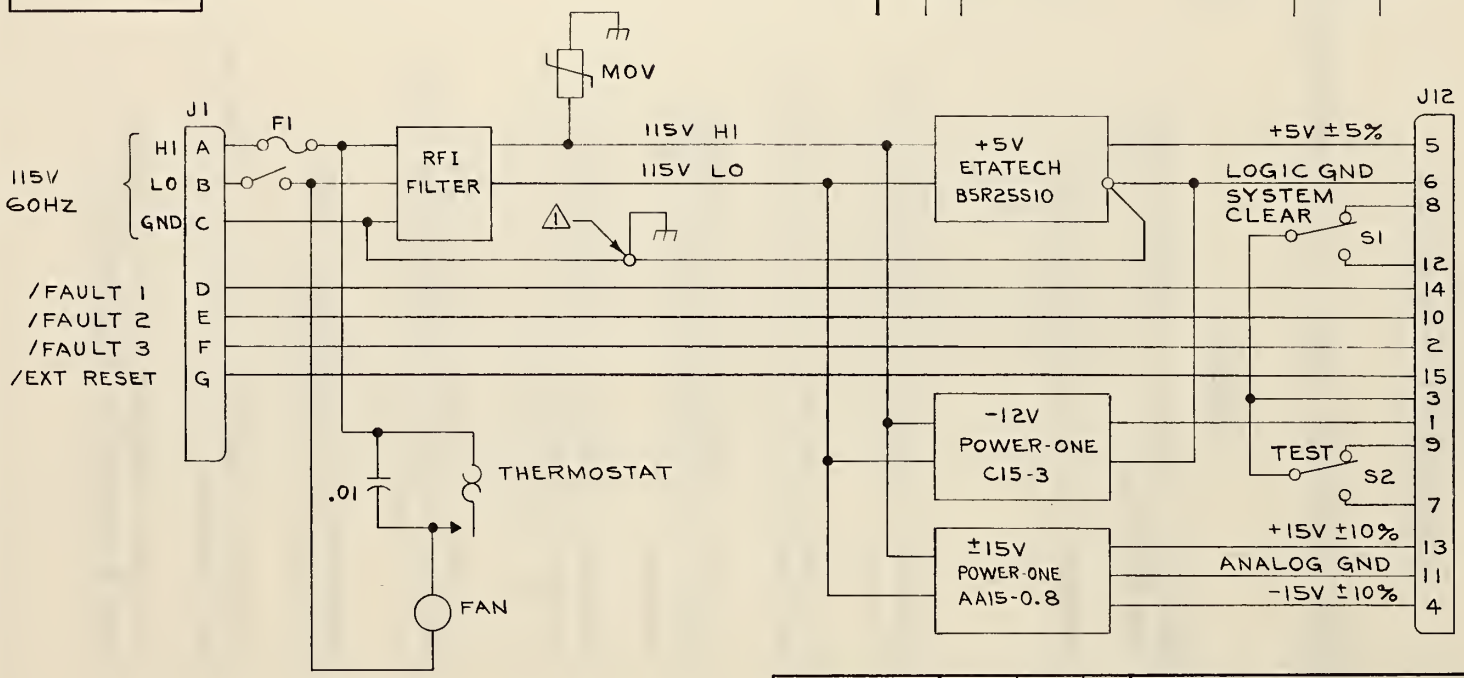
Drwg. No.	Subject	Revision
10059917	Schematic Diagram, Power Supply - Bus Detector	B
Signal List - BCU Backplane (Sheets 1 thru 6)	Motherboard Interconnect List	Original
10059899	Schematic Diagram - I/O Card, Bus Detector	G
10059900	Schematic Diagram - PROM Memory, Bus Detector	C
1059904 (Sheets 1, 2)	Schematic Diagram - Preprocessor Control Decoding Card No. 1, Bus Detector	E
10059901 (Sheet 1)	Schematic Diagram - Cycle Steal Control/Address, Preprocessor Card No. 2, Bus Detector	E
10059901 (Sheet 2)	Schematic Diagram - Cycle Steal Control/Address, Preprocessor Card No. 2, Bus Detector	D
10059923	Interconnecting Diagram - Loop Electronics, Bus Detector	C
10059903	Schematic Diagram - Loop Electronics, Bus Detector	
10059902	Schematic Diagram - Power Supply, Loop Electronics, Bus Detector	D

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM

HONEYWELL PART NO.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REV	6-20-77	
	B	REV	7-28-77	



⚠ GND LUG ON CHASSIS

TOLERANCES UNLESS NOTED OTHERWISE	
.X ±	90° FORMED ANGLES ±2° −1°
.XX ±	
.XXX ±	

FINISH—NOTE

MATL

NEXT ASSY	USED ON
APPLICATION	

DRAFTSMAN	J Jones	4-4-77
CHECK		
DEV ENGR		
PROJ ENGR		
RELIABILITY		

CONTRACT NO.

HONEYWELL INC. AEROSPACE AND DEFENSE GROUP

☐ AERO MPLS ☐ AERO ST PETERSBURG ☐ ORO SEATTLE ☐ ORO HOPKINS ☐ ORO MONTGOMERYVILLE ■ S&R CTR MPLS ☐ RADIATION CTR BOSTON

SCHEMATIC DIAGRAM
POWER SUPPLY
BUS DETECTOR

SIZE	CODE IDENT NO.	DRAWING NO.
B	27327	10059917

SCALE | WT | SHEET

DF-4 7-71 V600

MOTHER BOARD INTERCONNECT LIST

ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED	
GND	141-144 1-4 71, 72	1-4	1-4	1-4	1-4	1-4		(J12-4)
+5V	5-8 137-140	5-8	5-8	5-8	5-8	5-8		(J12-5)
+5V Batt.	9, 10							
SWØØ	12					12		
SWØ1	14					14		
SWØ2	13					13		
SWØ3	11					11		
SWØ4	24					24		
SWØ5	27					27		
SWØ6	68					68		
SWØ7	26					26		
SWØ8	76					76		
SWØ9	89					89		
SW1Ø	56					56		
SW11	53					53		
SW12	67					67		
SW13	84					84		
SW14	91					91		
SW15	70					70		
Flag Ø	15							
MDOØØ	35	35				35		
MDOØ1		49				49		
MDOØ2	17	17				17		
MDOØ3	21	21				21		
MDOØ4	42	42				42		
MDOØ5	45	45				45		
MDOØ6	18	18				18		
MDOØ7	22	22				22		
MDOØ8	25	25				25		
MDOØ9	38	38				38		
MDO1Ø	46	46				46		
MDO11	55	55				55		
MDO12	28	28				28		
MDO13	39	39				39		
MDO14	48	48				48		
MDO15	57	57				57		
-12V	31/32	31/32				31/32		(J12-3)
ODIS	44	44						
EXHOLD	122	121						

MOTHER BOARD INTERCONNECT LIST ORIGINAL NAME	CPU	P. MEM		PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED	
ADXØØ	63	63		63	63	63			
ADXØ1	86	86		86	86	86			
ADXØ2	88	88		88	88	88			
ADXØ3	85	85		85	85	85			
ADXØ4	64	64		64	64	64			
ADXØ5	62	62		62	62	62			
ADXØ6	65	65		65	65	65			
ADXØ7	66	66		66	66	66			
ADXØ8	60	60		60	60	60			
ADXØ9	50	50		50	50	50			
ADX1Ø	77	77		77	77	77			
ADX11	103	103		103	103	103			
ADX12	78	78		78	78	78			
ADX13	81	81		81	81	81			
ADX14	82	82		82	82	82			
ADX15	83	83		83	83	83			
CSØ*	61	61							Not Wired to DAYNL card
DSLCT	69			92		92			Tie to CPU, RDMF (92)
Flag 12									
CS1	79								Tie down (GND)
CS2	80								Tie Down (GND)
R/W*	87	87							
SEL	90								
RDMF	92			92		92			Tie also to CPU, DSLCT (69)
WRMF	93			93					
RDPF	94			94		94			
WRPF	95			95	95	95			Tie also to DEBUG, WRP (95)
F8	96				96	96			
HLT*	97					97			
BDOENA*	98	98							
F15									
CPINT	101	101				101			
F11	102				102				
C1	104								
CLK81	105			105		105			
DISTR*	106								
INCTCL		90				90			
C3B*									
C45	109			109	109	109			
CPINP	110					110			
F14	111								
EXEC	112	112				112			Called START on DAYNL
Power On*	113								Tie low
F13	114				114				

MOTHER BOARD INTERCONNECT LIST ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED	
WRPA	118							
C3	100							
INCTCLB	107	107						Called INCTCL on CPU
CLK	119							
WRMP	120	120						
CLK*	121			121				
EXHOLDS*		121		122				
RFREQ	123							Tie Low
RFSH	124							
WRPB	125							
CO	126							Connect to CPU CIN (128)
INTRA	127	127						
CIN	128							Connect to CPU CO (126)
JC12	129	129						
JC13	130							Tie Low
JC15	131				131			
F12								
JC14	133				133			
SYSCLR*	134				134			
INIT*	135				135	135		
INTEN	136	136				136		
BDØØØ	36			36	36	36		
BDØØ1	40			40	40	40		
BDØØ2	58			58	58	58		
BDØØ3	20			20	20	20		
BDØØ4	43			43	43	43		
BDØØ5	54			54	54	54		
BDØØ6	19			19	19	19		
BDØØ7	23			23	23	23		
BDØØ8	37			37	37	27		
BDØØ9	41			41	41	41		
BDØ1Ø	51			51	51	51		
BDØ11	52			52	52	52		
BDØ12	74			74	74	74		
BDØ13	73			73	73	73		
BDØ14	47			47	47	69		
BDØ15	59			59	59	59		
PPSTL*			24	24				
GMMDTAD*			25	25				
GMMADDD*			113	113				
GSTRTCV*			31	31				
GMEMLWRD*			111	111				
GMFMUPRD*			107	107				
GMARD*			104	104				
GCLKSTB*			28	28				
GMEMDEST*			30	30				
GMEMSRC*			32	32				

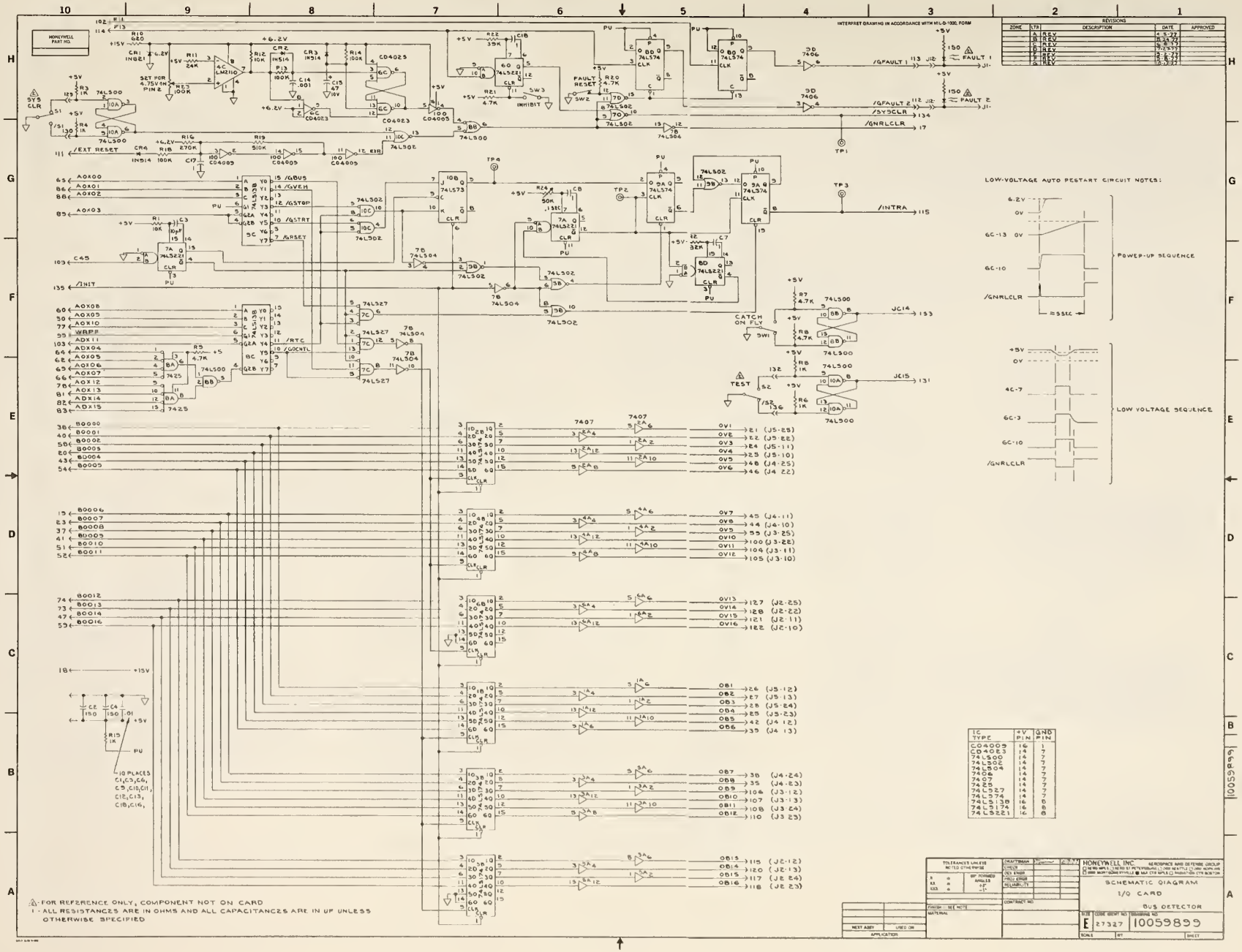
MOTHER BOARD INTERCONNECT LIST

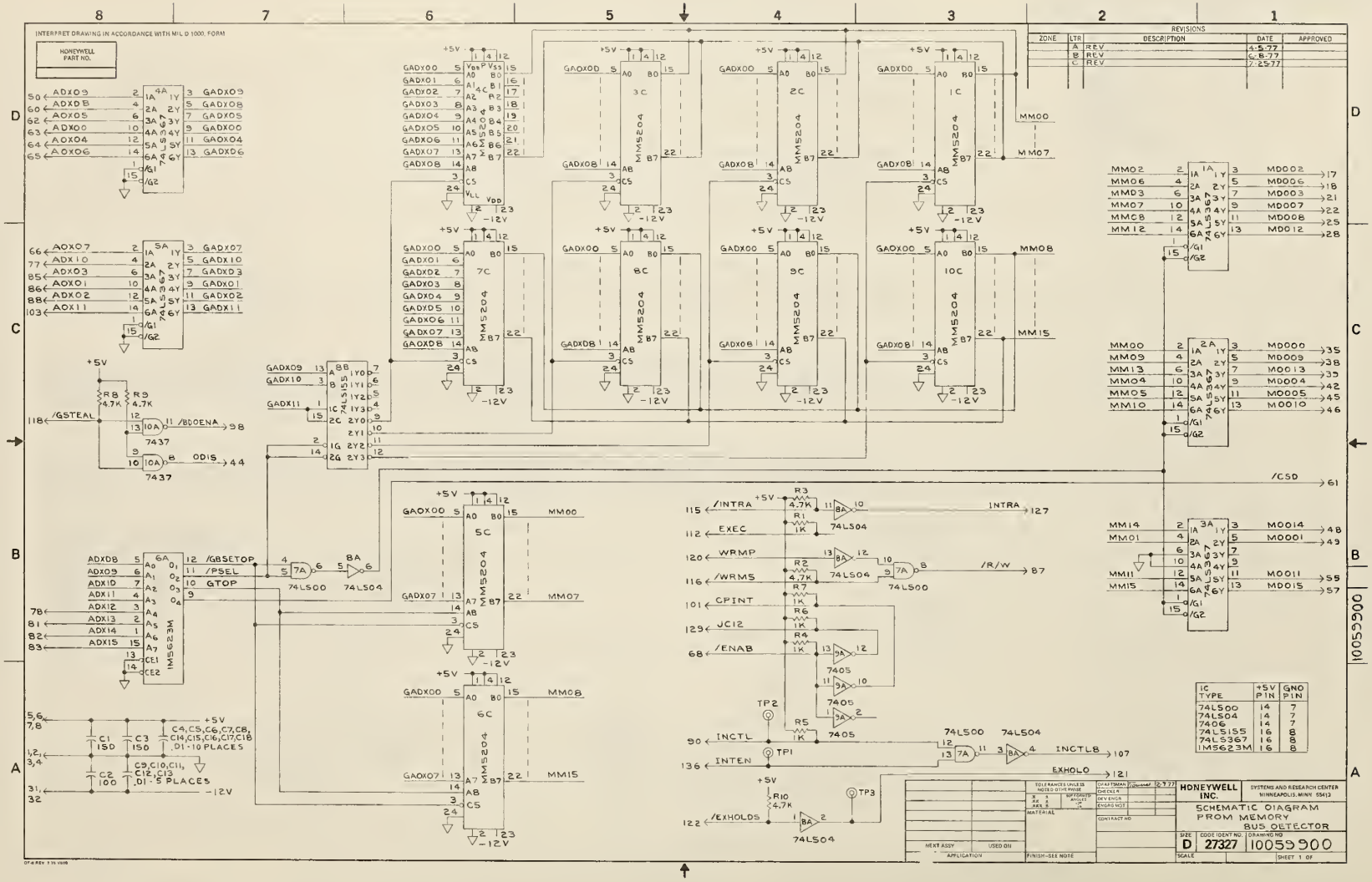
ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED	
GMEMUPRS*			34	34				
GADCONV*			29	29				
GMEMLWRS*			35	35				
GINCMAR*			106	106				
GDECMAR*			108	108				
GMARS*			110	110				
LSIGHI 1				9				To Connector J5-4
LSIGHI 2				13				To Connector J5-3
LSIGHI 3				10				To Connector J5-2
LSIGHI 4				14				To Connector J5-1
LSIGHI 5				46				To Connector J4-4
LSIGHI 6				55				To Connector J4-3
LSIGHI 7				67				To Connector J4-2
LSIGHI 8				68				To Connector J4-1
LSIGHI 9				87				To Connector J3-4
LSIGHI 10				90				To Connector J3-3
LSIGHI 11				96				To Connector J3-2
LSIGHI 12				97				To Connector J3-1
LSIGHI 13				117				To Connector J2-4
LSIGHI 14				123				To Connector J2-3
LSIGHI 15				125				To Connector J2-2
LSIGHI 16				127				To Connector J2-1
LSIGLO 1				11				To Connector J5-17
LSIGLO 2				15				To Connector J5-16
LSIGLO 3				12				To Connector J5-15
LSIGLO 4				16				To Connector J5-14
LSIGLO 5				48				To Connector J4-17
LSIGLO 6				57				To Connector J4-16
LSIGLO 7				69				To Connector J4-15
LSIGLO 8				70				To Connector J4-14
LSIGLO 9				89				To Connector J3-17
LSIGLO 10				91				To Connector J3-16
LSIGLO 11				98				To Connector J3-15
LSIGLO 12				99				To Connector J3-14
LSIGLO 13				119				To Connector J2-17
LSIGLO 14				124				To Connector J2-16
LSIGLO 15				126				To Connector J2-15
LSIGLO 16				128				To Connector J2-14
PGS*								
/PPSTLP			112	112				
BPPDØ			46	45				
BPPD1			50	49				
BPPD2			53	53				
BPPD3			56	56				
BPPD4			61	61				
BPPD5			75	75				

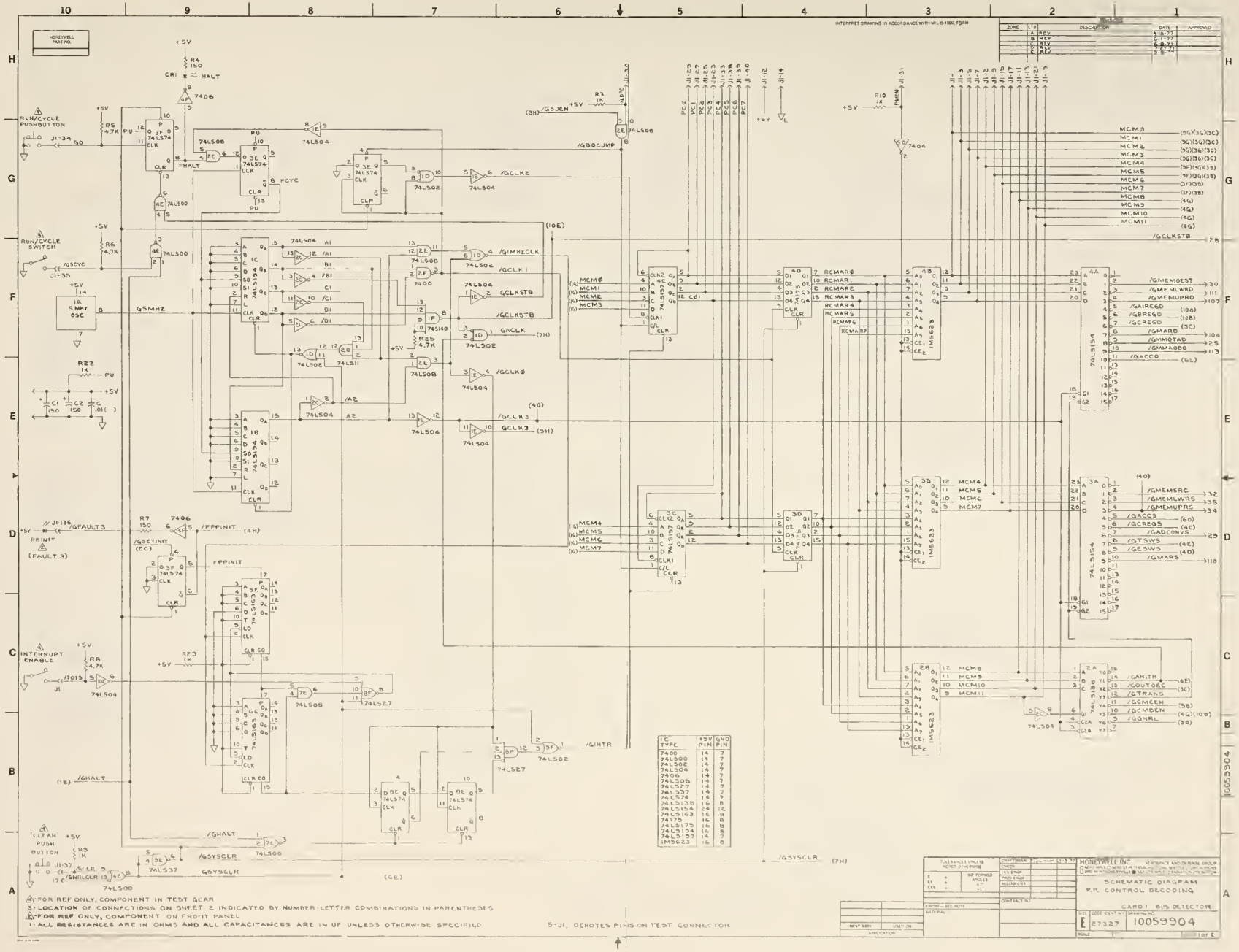
MOTHER BOARD INTERCONNECT LIST ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED	
BPPD6			76	76				
BPPD7			79	79				
BPPD8			80	80				
BPPD9			100	100				
BPPD10			101	102				
BPPD11			102	101				
ENAB*		68				69		Gnd by DAYNL
INTRA*		115			115			
WRMS*		116		116				
ASC2*								
CS0*								Not wired to CPU
CS2*								Tied High
CS1*								Tied High
CS3*								
RDM						92		Connect to CPU, RDMF (92)
RDP								Connect to CPU, RDPF (94)
WRP						95		Connect to CPU, WRPF (95)
START								Connect to CPU, EXEC (112)
+15V				18	18			J12-15
-15V				136				J12-6
GNRLCLR*			17		17			
S1					129			To Front Panel (J12-8)
S1*					130			To Front Panel (J12-10)
S2					132			To Front Panel (J12-7)
S2*					136			To Front Panel (J12-9)
OV1					21			To Connector J5-25
OV2					22			To Connector J5-22
OV3					24			To Connector J5-11
OV4					25			To Connector J5-10
OV5					48			To Connector J4-25
OV6					46			To Connector J4-22
OV7					45			To Connector J4-11
OV8					44			To Connector J4-10
OV9					99			To Connector J3-25
OV10					100			To Connector J3-22
OV11					104			To Connector J3-11
OV12					105			To Connector J3-10
OV13					127			To Connector J2-25
OV14					128			To Connector J2-22
OV15					121			To Connector J2-11
OV16					122			To Connector J2-10
OB1					26			To Connector J5-12
OB2					27			To Connector J5-13
OB3					28			To Connector J5-24
OB4					29			To Connector J5-23
OB5					42			To Connector J4-12

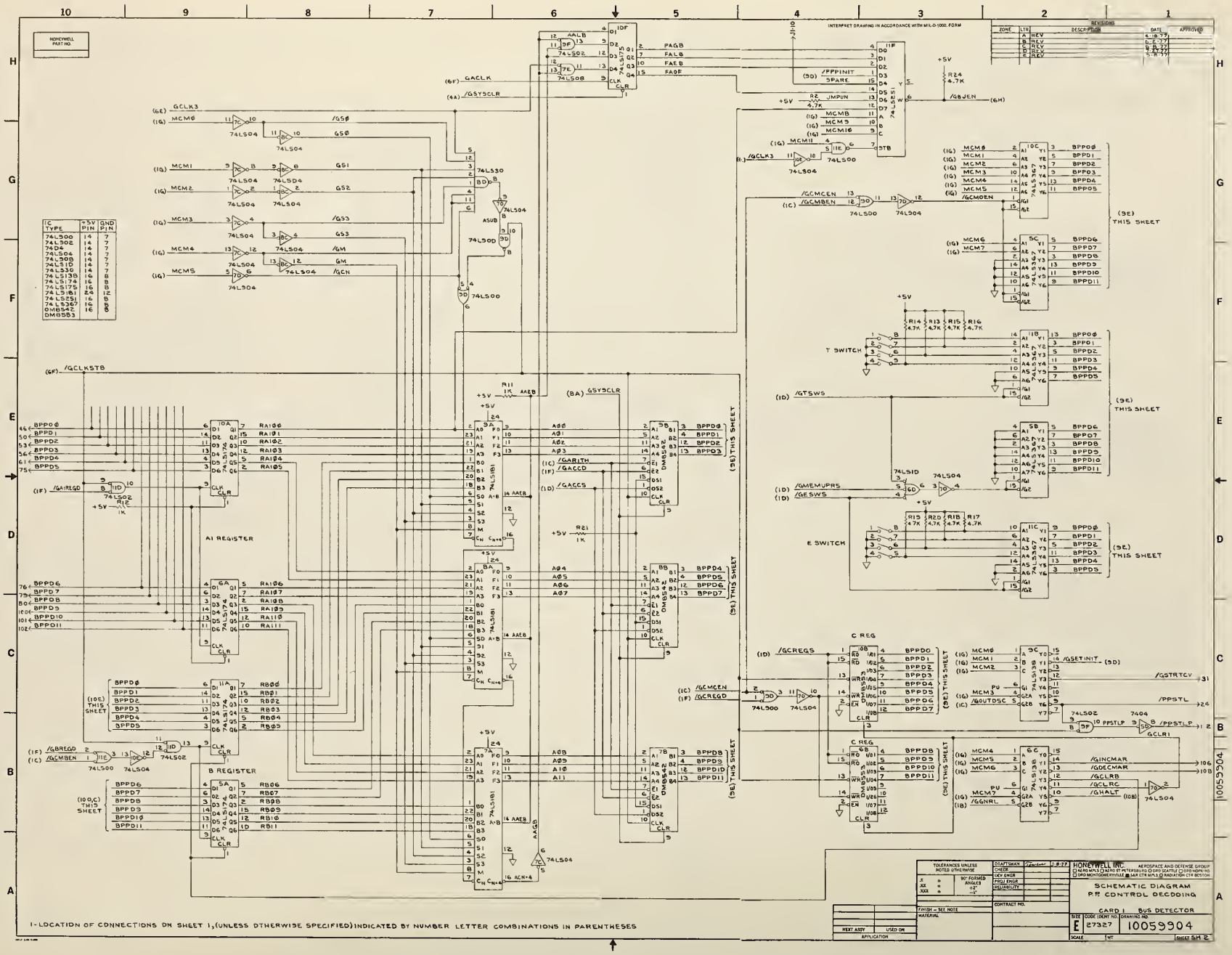
MOTHER BOARD INTERCONNECT LIST

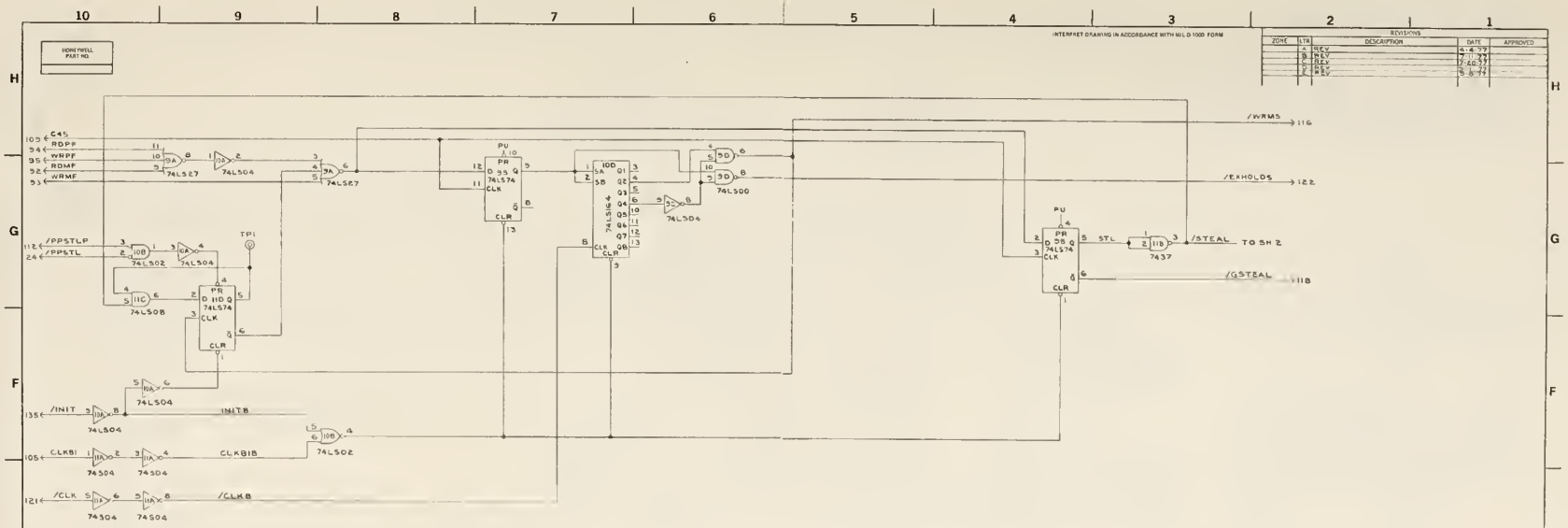
ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED	
OB6					39			To Connector J4-13
OB7					38			To Connector J4-24
OB8					35			To Connector J4-23
OB9					106			To Connector J3-12
OB10					107			To Connector J3-13
OB11					108			To Connector J3-24
OB12					110			To Connector J3-23
OB13					119			To Connector J2-12
OB14					120			To Connector J2-13
OB15					117			To Connector J2-24
OB16					118			To Connector J2-23
ANALOG GND								From Power Supply (J12)
/GFAULT 1					113			CR1 & J12-14
/GFAULT 2					112			CR2 & J12-12
/GFAULT 3			136					CR3 & J12-2
/EXT RESET					111			To Connector J12-13
LOGIC GND								To Connector J12-1
/GSTEAL		118		118				
SIG SHIELD								To Connector Pins J2-5 J3-5, J4-5, J5-5


HONEYWELL PART NO.
INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A REV 4-5-77
B REV 5-24-77
C REV 6-8-77
D REV 4-29-77
E REV 5-6-77
F REV 5-6-77
G REV 8-3-77
/GFAULT 1
/GFAULT 2
/SYSCLR
/GNRLCLR
/INTRA
/GBUS
/GVEH
/GSTOP
/GSTRT
/GRSET
/INIT
/RTC
/LOCNTL
/EXT RESET
SET POR 4.75V ON PIN 2
INHIBIT
FAULT RESET
CATCH ON FLY
TEST
LOW-VOLTAGE AUTO RESTART CIRCUIT NOTES:
POWER-UP SEQUENCE
LOW VOLTAGE SEQUENCE
10 PLACES C1,C3,C6,C9,C10,C11,C12,C13,C18,C19,
IC TYPE | +V PIN | GND PIN
CD4009 | 16 | 1
CD4023 | 14 | 7
74LS00 | 14 | 7
74LS02 | 14 | 7
74LS04 | 14 | 7
7406 | 14 | 7
7407 | 14 | 7
7425 | 14 | 7
74LS27 | 14 | 7
74LS74 | 14 | 7
74LS138 | 16 | 8
74LS174 | 16 | 8
74LS221 | 16 | 8
FOR REFERENCE ONLY, COMPONENT NOT ON CARD
1. ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN UF UNLESS OTHERWISE SPECIFIED
HONEYWELL INC.
SCHEMATIC DIAGRAM
I/O CARD
BUS DETECTOR
SIZE E
CODE IDENT NO. 27327
DRAWING NO. 10059899
SCALE
WT
SHEET
NEXT ASSY
USED ON
APPLICATION
10059899


INTERPRET DRAWING IN ACCORDANCE WITH MIL D 1000, FORM
HONEYWELL PART NO.
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A REV 4-5-77
B REV 6-8-77
C REV 7-25-77
74LS367
74LS155
MM5204
IM5623M
74LS00
74LS04
7437
7405
/GSTEAL
/BDOENA
ODIS
/GBSETOP
/PSEL
GTOP
/INTRA
EXEC
WRMP
/WRMS
CPINT
JC12
/ENAB
INCTL
INTEN
/EXHOLDS
INTRA
/R/W
INCTLB
EXHOLD
/CSD
IC TYPE +5V PIN GND PIN
74LS00 14 7
74LS04 14 7
7406 14 7
74LS155 16 8
74LS367 16 8
IM5623M 16 8
HONEYWELL INC.
SYSTEMS AND RESEARCH CENTER
MINNEAPOLIS, MINN 55413
SCHEMATIC DIAGRAM
PROM MEMORY
BUS DETECTOR
SIZE D
CODE IDENT NO. 27327
DRAWING NO 10059900
SHEET 1 OF
10059900


INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM
HONEYWELL PART NO.
RUN/CYCLE PUSHBUTTON
RUN/CYCLE SWITCH
INTERRUPT ENABLE
'CLEAN' PUSH BUTTON
1A 5 MHZ OSC
GSMHZ
/GFAULT3
RPINIT
(FAULT 3)
/GSETINIT (2C)
FPPINIT
/GSYSCLR
/GHALT
/GINTR
/GBOCJMP
/GIMHZCLK
/GCLK1
/GCLKSTB
/GACLK
/GCLKØ
/GCLK2
/GCLK3
/GCLKSTB
/GMEMOEST
/GMEMLWRD
/GMEMUPRD
/GAIREGD
/GBREGD
/GCREGD
/GMARD
/GMMOTAD
/GMMAODD
/GACCD
/GMEMSRC
/GMEMLWRS
/GMEMUPRS
/GACCS
/GCREGS
/GADCONVS
/GTSWS
/GESWS
/GWARS
/GARITH
/GOUTOSC
/GTRANS
/GCMCEN
/GCMBEN
/GGNRL
MCMØ
MCM1
MCM2
MCM3
MCM4
MCM5
MCM6
MCM7
MCMØ
MCM1
MCM2
MCM3
MCM4
MCM5
MCM6
MCM7
MCM8
MCM9
MCM10
MCM11
RCMARØ
RCMAR1
RCMAR2
RCMAR3
RCMAR4
RCMAR5
RCMAR6
RCMAR7
IC TYPE | +5V PIN | GND PIN
7400 | 14 | 7
74LS00 | 14 | 7
74LS02 | 14 | 7
74LS04 | 14 | 7
7406 | 14 | 7
74LS08 | 14 | 7
74LS27 | 14 | 7
74LS37 | 14 | 7
74LS74 | 14 | 7
74LS139 | 16 | 8
74LS154 | 24 | 12
74LS163 | 16 | 8
74175 | 16 | 8
74LS175 | 16 | 8
74LS194 | 16 | 8
74LS157 | 14 | 7
IM5623 | 16 | 8
1- ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN UF UNLESS OTHERWISE SPECIFIED
5- J1, DENOTES PINS ON TEST CONNECTOR
HONEYWELL INC
SCHEMATIC DIAGRAM
P.P. CONTROL DECODING
CARD 1 B/S DETECTOR
SIZE E
CODE IDENT NO 27327
DRAWING NO 10059904
SCALE
SHEET 1 OF 2

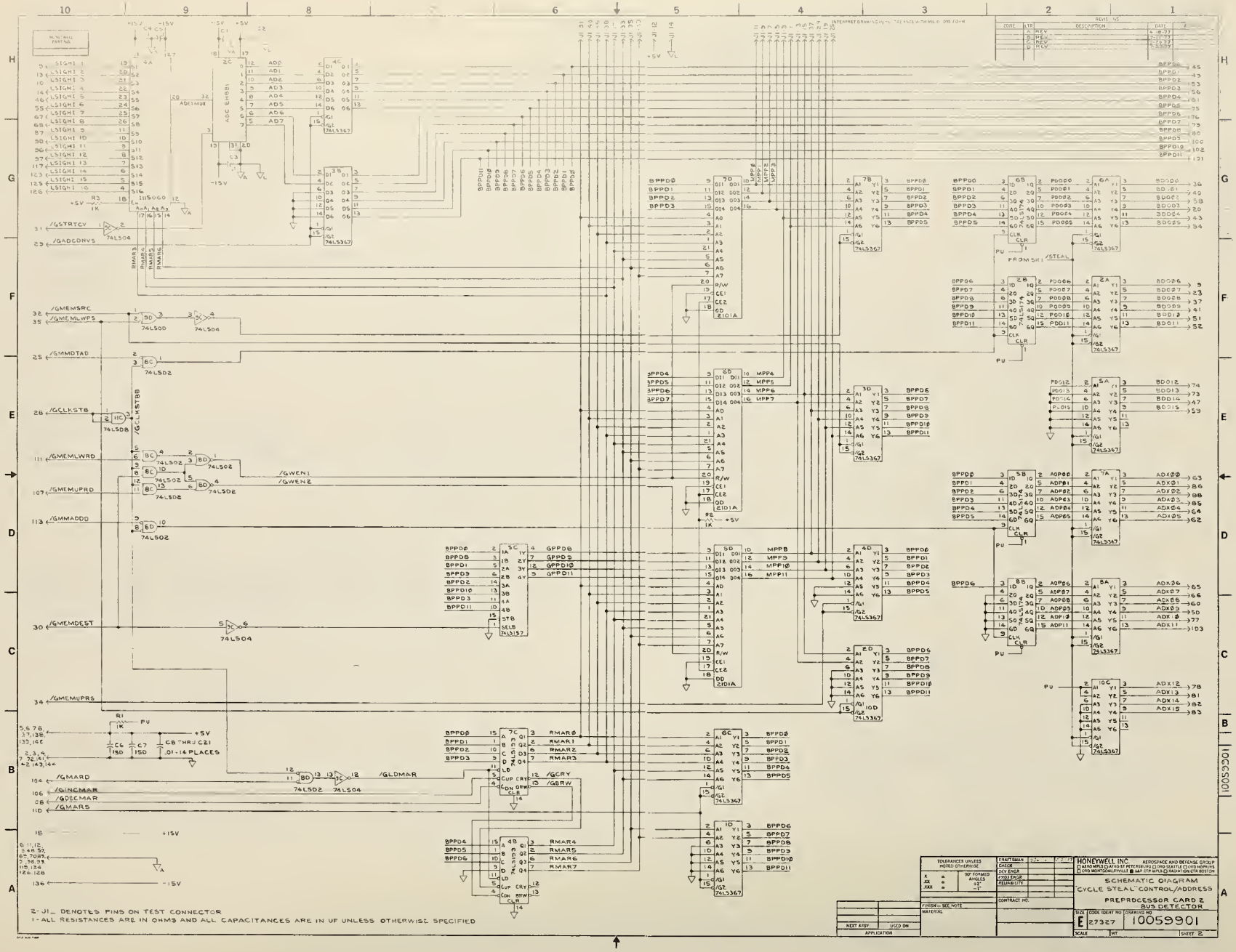

HONEYWELL PART NO.
INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A REV 4-18-77
B REV 6-2-77
C REV 8-8-77
D REV 8-8-77
E REV 11-18-77
IC TYPE +5V PIN GND PIN
74LS00 14 7
74LS02 14 7
74D4 14 7
74LS04 14 7
74LS08 14 7
74LS10 14 7
74LS30 14 7
74LS138 16 8
74LS174 16 8
74LS175 16 8
74LS181 24 12
74LS251 16 8
74LS367 16 8
DM8542C 16 8
DM8583 8
A1 REGISTER
B REGISTER
C REG
T SWITCH
E SWITCH
THIS SHEET
SCHEMATIC DIAGRAM
P.P. CONTROL DECODING
CARD 1 BUS DETECTOR
HONEYWELL INC.
AEROSPACE AND DEFENSE GROUP
SIZE E CODE IDENT NO. 27327 DRAWING NO. 10059904
SHEET SH 2
1-LOCATION OF CONNECTIONS ON SHEET 1, (UNLESS OTHERWISE SPECIFIED) INDICATED BY NUMBER LETTER COMBINATIONS IN PARENTHESES
10059904

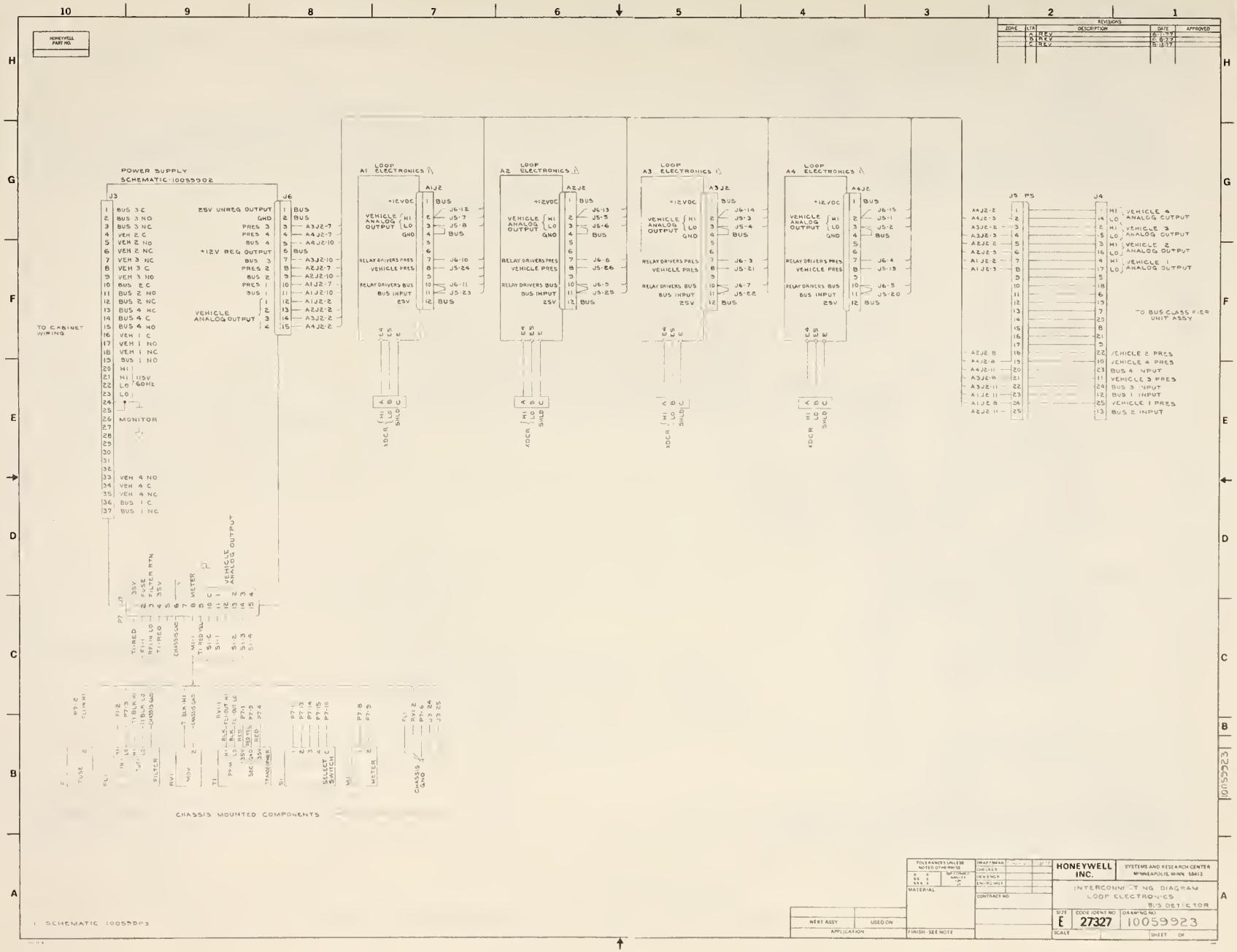


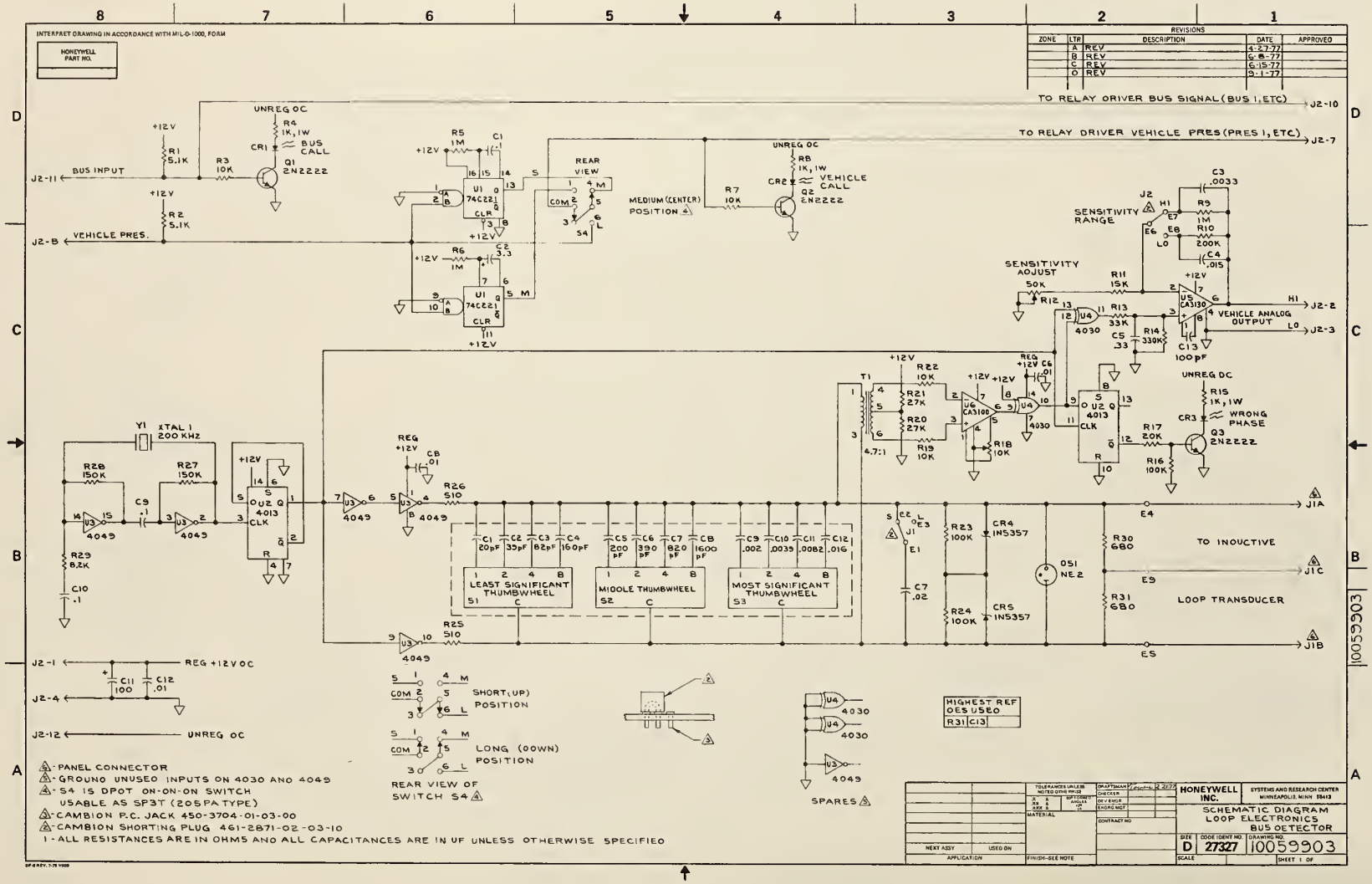
IC TYPE	+5V PIN	GND PIN
74LS00	14	7
74LS02	14	7
74S04	14	7
74LS04	14	7
74LS08	14	7
74LS27	14	7
7437	14	7
74LS374	14	7
74LS157	16	8
74164	14	7
74LS174	16	8
74LS193	16	8
74LS367	16	8
E101A	22	8

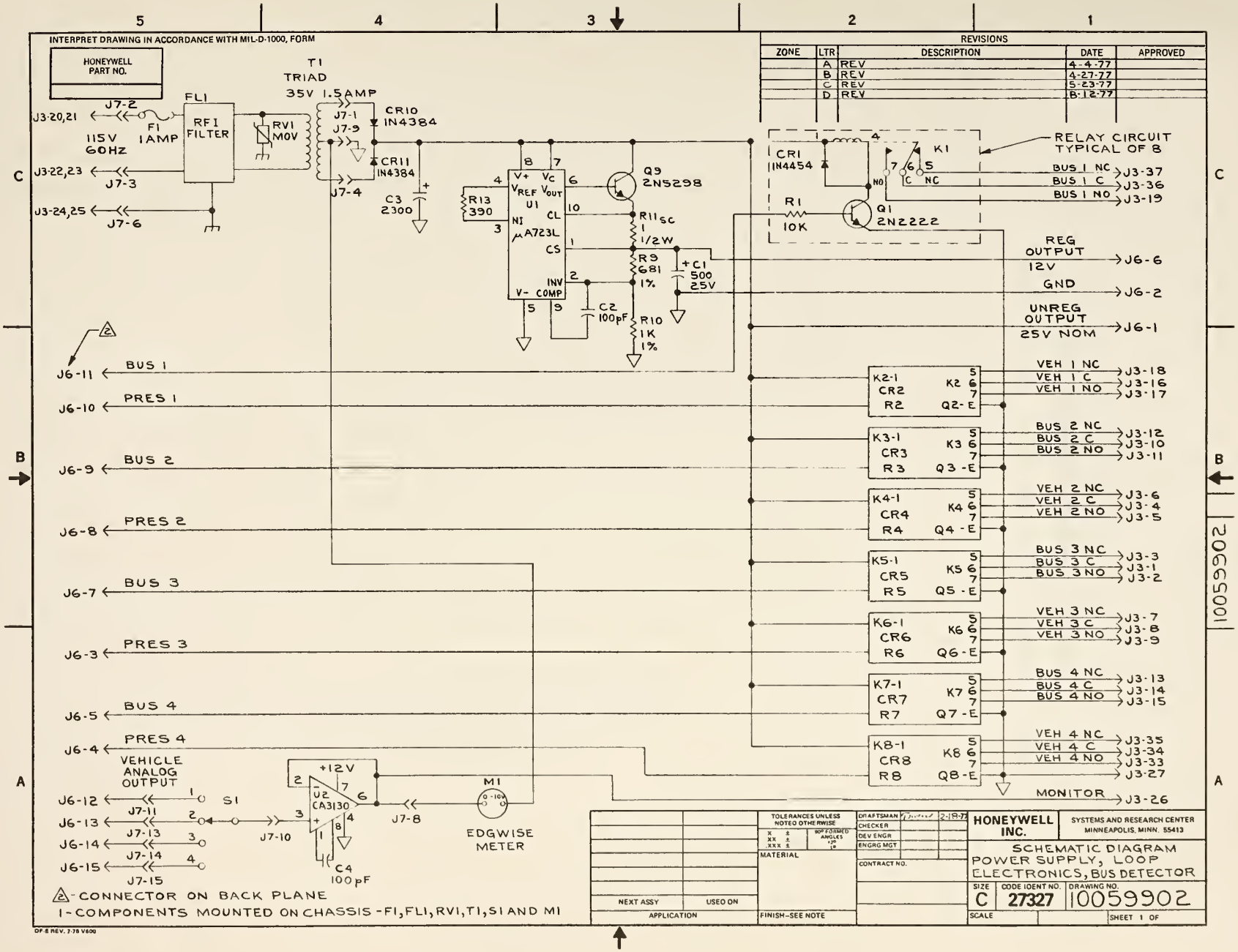
POLERANCES UNLESS NOTED OTHERWISE
DRAFTSMAN
CHECK
DESIGN ENGR
RELIABILITY
CONTRACT NO
FINISH - SEE NOTE
MATERIAL
NEXT ASSY
USED ON
APPLICATION

HONEYWELL INC
SCHEMATIC DIAGRAM
CYCLE STEAL CONTROL/ADDRESS
PREPROCESSOR CARDS
BUS DETECTOR
SIZE E
CODE IDENT NO 27327
DRAWING NO 10059901
SHEET 1 OF 2


HONEYWELL INC.
AEROSPACE AND DEFENSE GROUP
SCHEMATIC DIAGRAM
"CYCLE STEAL" CONTROL/ADDRESS
PREPROCESSOR CARD 2
BUS DETECTOR
E
27327
10059901
SHEET 2
2-J1_ DENOTES PINS ON TEST CONNECTOR
1-ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN UF UNLESS OTHERWISE SPECIFIED


HONEYWELL PART NO.
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A REV 6-1-77
B REV 7-6-77
C REV 8-12-77
POWER SUPPLY
SCHEMATIC-10055902
J3
J6
25V UNREG OUTPUT
GND
PRES 3
PRES 4
BUS 4
+12V REG OUTPUT
BUS 3
PRES 2
BUS 2
PRES 1
BUS 1
VEHICLE ANALOG OUTPUT
TO CABINET WIRING
MONITOR
115V 60HZ
LOOP ELECTRONICS A1
LOOP ELECTRONICS A2
LOOP ELECTRONICS A3
LOOP ELECTRONICS A4
+12VDC
VEHICLE ANALOG OUTPUT
RELAY DRIVERS PRES
VEHICLE PRES
RELAY DRIVERS BUS
BUS INPUT
25V
BUS
J5 P5
J4
VEHICLE 4 ANALOG OUTPUT
VEHICLE 3 ANALOG OUTPUT
VEHICLE 2 ANALOG OUTPUT
VEHICLE 1 ANALOG OUTPUT
TO BUS CLASSIFIER UNIT ASSY
VEHICLE 2 PRES
VEHICLE 4 PRES
BUS 4 INPUT
VEHICLE 3 PRES
BUS 3 INPUT
BUS 1 INPUT
VEHICLE 1 PRES
BUS 2 INPUT
CHASSIS MOUNTED COMPONENTS
SCHEMATIC 10055903
TOLERANCES UNLESS NOTED OTHERWISE
MATERIAL
FINISH SEE NOTE
NEXT ASSY
USED ON
APPLICATION
CONTRACT NO.
HONEYWELL INC.
SYSTEMS AND RESEARCH CENTER
MINNEAPOLIS, MINN. 55413
INTERCONNECTING DIAGRAM
LOOP ELECTRONICS
BUS DETECTOR
SIZE E
CODE IDENT NO. 27327
DRAWING NO. 10059923
SCALE
SHEET OF
10059923


INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM
HONEYWELL PART NO.
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A REV 4-27-77
B REV 5-18-77
C REV 6-15-77
D REV 9-1-77
TO RELAY DRIVER BUS SIGNAL (BUS 1, ETC) J2-10
TO RELAY DRIVER VEHICLE PRES (PRES 1, ETC) J2-7
UNREG DC
R4 1K, 1W
CR1 BUS CALL
Q1 2N2222
+12V
R1 5.1K
R3 10K
J2-11 BUS INPUT
R2 5.1K
J2-8 VEHICLE PRES.
R5 1M
C1 .1
U1 74C221
CLR
R6 1M
C2 3.3
REAR VIEW
COM
S4
MEDIUM (CENTER) POSITION 4
R7 10K
R8 1K, 1W
CR2 VEHICLE CALL
Q2 2N2222
C3 .0033
R9 1M
R10 200K
C4 .015
SENSITIVITY RANGE
SENSITIVITY ADJUST
50K R12
R11 15K
U5 CA3130
U4 4030
R13 33K
R14 330K
C5 .33
C13 100 pF
H1 J2-2
LO J2-3
VEHICLE ANALOG OUTPUT
UNREG DC
R15 1K, 1W
CR3 WRONG PHASE
Q3 2N2222
R16 100K
R17 20K
U2 4013
CLK
T1
4.7:1
R22 10K
R21 27K
R20 27K
R19 10K
U6 CA3100
R18 10K
REG +12V C6 .01
Y1 XTAL 1 200 KHZ
R28 150K
R27 150K
C9 .1
U3 4049
R29 8.2K
C10 .1
REG +12V
C8 .01
R26 510
R25 510
C1 20pF
C2 35pF
C3 82pF
C4 160pF
LEAST SIGNIFICANT THUMBWHEEL
S1
C5 200 pF
C6 390 pF
C7 820 pF
C8 1600 pF
MIDDLE THUMBWHEEL
S2
C9 .002
C10 .0039
C11 .0082
C12 .016
MOST SIGNIFICANT THUMBWHEEL
S3
J1A
J1C
J1B
E4
E9
E5
J1
E1
E2
E3
C7 .02
R23 100K
R24 100K
CR4 1N5357
CR5 1N5357
051 NE2
R30 680
R31 680
TO INDUCTIVE
LOOP TRANSDUCER
J2-1 REG +12V DC
J2-4
C11 100
C12 .01
J2-12 UNREG DC
SHORT (UP) POSITION
LONG (DOWN) POSITION
REAR VIEW OF SWITCH S4 4
SPARES 5
HIGHEST REF DES USED
R31 C13
1 PANEL CONNECTOR
2 GROUND UNUSED INPUTS ON 4030 AND 4049
3 S4 IS DPDT ON-ON-ON SWITCH USABLE AS SP3T (205PA TYPE)
4 CAMBION P.C. JACK 450-3704-01-03-00
5 CAMBION SHORTING PLUG 461-2871-02-03-10
1-ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN UF UNLESS OTHERWISE SPECIFIED
HONEYWELL INC.
SYSTEMS AND RESEARCH CENTER
MINNEAPOLIS, MINN 55413
SCHEMATIC DIAGRAM
LOOP ELECTRONICS
BUS DETECTOR
SIZE D
CODE IDENT NO. 27327
DRAWING NO. 10059903
SCALE
SHEET 1 OF
10059903


INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM
HONEYWELL PART NO.
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A REV 4-4-77
B REV 4-27-77
C REV 5-23-77
D REV 8-12-77
J3-20,21
J7-2
F1 1AMP
115V 60HZ
J3-22,23
J7-3
J3-24,25
J7-6
FL1
RFI FILTER
RV1 MOV
T1 TRIAD 35V 1.5AMP
J7-1
J7-9
J7-4
CR10 1N4384
CR11 1N4384
C3 2300
R13 390
U1 μA723L
Q9 2N5298
R11 1 1/2W
R9 681 1%
C1 500 25V
C2 100pF
R10 1K 1%
CR1 1N4454
K1
R1 10K
Q1 2N2222
RELAY CIRCUIT TYPICAL OF 8
BUS 1 NC J3-37
BUS 1 C J3-36
BUS 1 NO J3-19
REG OUTPUT 12V J6-6
GND J6-2
UNREG OUTPUT 25V NOM J6-1
J6-11 BUS 1
J6-10 PRES 1
J6-9 BUS 2
J6-8 PRES 2
J6-7 BUS 3
J6-3 PRES 3
J6-5 BUS 4
J6-4 PRES 4
VEHICLE ANALOG OUTPUT
J6-12
J6-13
J6-14
J6-15
J7-11
J7-13
J7-14
J7-15
S1
J7-10
U2 CA3130
+12V
C4 100pF
J7-8
M1 0-10V
EDGWISE METER
K2-1 CR2 R2 K2 Q2-E
VEH 1 NC J3-18
VEH 1 C J3-16
VEH 1 NO J3-17
K3-1 CR3 R3 K3 Q3-E
BUS 2 NC J3-12
BUS 2 C J3-10
BUS 2 NO J3-11
K4-1 CR4 R4 K4 Q4-E
VEH 2 NC J3-6
VEH 2 C J3-4
VEH 2 NO J3-5
K5-1 CR5 R5 K5 Q5-E
BUS 3 NC J3-3
BUS 3 C J3-1
BUS 3 NO J3-2
K6-1 CR6 R6 K6 Q6-E
VEH 3 NC J3-7
VEH 3 C J3-8
VEH 3 NO J3-9
K7-1 CR7 R7 K7 Q7-E
BUS 4 NC J3-13
BUS 4 C J3-14
BUS 4 NO J3-15
K8-1 CR8 R8 K8 Q8-E
VEH 4 NC J3-35
VEH 4 C J3-34
VEH 4 NO J3-33
J3-27
MONITOR J3-26
2-CONNECTOR ON BACK PLANE
1-COMPONENTS MOUNTED ON CHASSIS-F1,FL1,RV1,T1,S1 AND M1
NEXT ASSY USED ON
APPLICATION
TOLERANCES UNLESS NOTED OTHERWISE
MATERIAL
FINISH-SEE NOTE
DRAFTSMAN
CHECKER
DEV ENGR
ENGRG MGT
CONTRACT NO.
HONEYWELL INC.
SYSTEMS AND RESEARCH CENTER MINNEAPOLIS, MINN. 55413
SCHEMATIC DIAGRAM POWER SUPPLY, LOOP ELECTRONICS, BUS DETECTOR
SIZE C
CODE IDENT NO. 27327
DRAWING NO. 10059902
SCALE
SHEET 1 OF
OF-8 REV. 7-75 V600

APPENDIX
IMP-16C APPLICATIONS MANUAL

See Volume II.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1978— 621-678/296

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U.S. FEDE
ADMINIST

REPORT NO

Form DOT F 172
FORMERLY FORM DO

FEDERALLY COORDINATED PROGRAM OF HIGHWAY RESEARCH AND DEVELOPMENT (FCP)

The Offices of Research and Development of the Federal Highway Administration are responsible for a broad program of research with resources including its own staff, contract programs, and a Federal-Aid program which is conducted by or through the State highway departments and which also finances the National Cooperative Highway Research Program managed by the Transportation Research Board. The Federally Coordinated Program of Highway Research and Development (FCP) is a carefully selected group of projects aimed at urgent, national problems, which concentrates these resources on these problems to obtain timely solutions. Virtually all of the available funds and staff resources are a part of the FCP, together with as much of the Federal-aid research funds of the States and the NCHRP resources as the States agree to devote to these projects.*

FCP Category Descriptions

1. Improved Highway Design and Operation for Safety

Safety R&D addresses problems connected with the responsibilities of the Federal Highway Administration under the Highway Safety Act and includes investigation of appropriate design standards, roadside hardware, signing, and physical and scientific data for the formulation of improved safety regulations.

2. Reduction of Traffic Congestion and Improved Operational Efficiency

Traffic R&D is concerned with increasing the operational efficiency of existing highways by advancing technology, by improving designs for existing as well as new facilities, and by keeping the demand-capacity relationship in better balance through traffic management techniques such as bus and carpool preferential treatment, motorist information, and rerouting of traffic.

3. Environmental Considerations in Highway Design, Location, Construction, and Operation

Environmental R&D is directed toward identifying and evaluating highway elements which affect the quality of the human environment. The ultimate goals are reduction of adverse highway and traffic impacts, and protection and enhancement of the environment.

4. Improved Materials Utilization and Durability

Materials R&D is concerned with expanding the knowledge of materials properties and technology to fully utilize available naturally occurring materials, to develop extender or substitute materials for materials in short supply, and to devise procedures for converting industrial and other wastes into useful highway products. These activities are all directed toward the common goals of lowering the cost of highway construction and extending the period of maintenance-free operation.

5. Improved Design to Reduce Costs, Extend Life Expectancy, and Insure Structural Safety

Structural R&D is concerned with furthering the latest technological advances in structural designs, fabrication processes, and construction techniques, to provide safe, efficient highways at reasonable cost.

6. Prototype Development and Implementation of Research

This category is concerned with developing and transferring research and technology into practice, or, as it has been commonly identified, "technology transfer."

7. Improved Technology for Highway Maintenance

Maintenance R&D objectives include the development and application of new technology to improve management, to augment the utilization of resources, and to increase operational efficiency and safety in the maintenance of highway facilities.

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* The complete 7-volume official statement of the FCP is available from the National Technical Information Service (NTIS), Springfield, Virginia 22161 (Order No. PB 242057, price $45 postpaid). Single copies of the introductory volume are obtainable without charge from Program Analysis (HRD-2), Offices of Research and Development, Federal Highway Administration, Washington, D.C. 20590.

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